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DESIGN AND SIMULATION OF A GAAS SECOND ORDER SIGMA-DELTA A/D CONVERTER

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AUGUST 1993

FINAL REPORT FOR 01/01/93-08/01/93

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13. ABSTRACT *(Maximum 200 words)* In this report, the design and simulation of a sigma–delta analog–to–digital converter is presented. The key to sigma–delta conversion is trading off time resolution for amplitude resolution. In this report, second–order converters are used which allows the amplitude resolution to increase several times faster than the time resolution decreases. The sigma–delta modulator contains two basic components—an analog sigma–delta modulator and a digital low–pass filter. The modulator generates a stream of bits representing the analog input. The low–pass filter takes out the high frequency variations in this bit stream and generates a stream of multi–bit words. The report shows the designs and simulations of two different second–order sigma–delta modulators. Both of these circuits use Gallium–Arsenide MESFET technology to achieve an oversampled clock rate of 512–MHz. The first modulator contains unique integrators based on the square law of field effect transistors (FETSs). The second modulator contains integrators using single–stage op–amps, current sources, and current sinks. Both modulators contain a unique clocking scheme that allows the continuous–time integrators to be insensitive to the delay of the quantizers. The filter presented in this thesis is simulated behaviorally. It contains multiple stages. One of these stages is a very simple averaging filter which allows good noise attenuation for sigma–delta modulators. The final output of the filter has a precision of 9–10 bits for a bandwidth of 8 MHz. The final output of the filter has a precision of 9–10 bits for a Nyquist rate of 16 MHz.

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Abstract

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The high accuracy of digital processors is becoming very important in the field of signal processing. Digital processing is so much more accurate than analog processing because of its large margins for voltage and component variations. In digital signal processing, the precision of the digital processor usually does not the limit the complete signal processing cycle. Modern digital processors can get a precision of 64 bits in a single clock cycle. The bottleneck is usually the analog-to-digital converter and sometimes the digital-to-analog converters. Many times, it may be difficult to achieve more than 8 bits of resolution for an analog-to-digital converter because of the need for many accurate analog components.

In this thesis, the design and simulation of a sigma-delta analog-to-digital converter is presented. This type of analog-to-digital converter does not need the high degree of analog component matching as does other analog-to-digital converters. The key to sigma-delta conversion is trading off time resolution for amplitude resolution. In this thesis, second-order converters are used which allows the amplitude resolution to increase several times faster than the time resolution decreases. The sigma-delta analog-to-digital converter contains two basic components - analog sigma-delta modulator and digital low-pass filter. The modulator generates a stream of bits representing the analog input. The low-pass filter takes out the high frequency variations in this bit stream and generates a stream of multi-bit words.

This thesis shows the designs and simulations of two different second-order sigma-delta modulators. Both of these circuits use Gallium-Arsenide MESFET technology to achieve an oversampled clock rate of 512-MHz. The first modulator contains unique integrators based on the square law of field effect transistors (FETs). The second modulator contains integrators using single-stage op-amps, current sources, and current

sinks. Both modulators contain a unique clocking scheme that allows the continuous-time integrators to be insensitive to the delay of the quantizers. Both of these modulators are able to be modeled in discrete-time even though continuous-time integrators are used.

The filter presented in this thesis is simulated behaviorally. It contains multiple stages. One of these stages is a very simple averaging filter which allows good noise attenuation for sigma-delta modulators. The final output of the filter has a precision of 9-10 bits for a Nyquist rate of 16 MHz.

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1. Introduction

An analog-to-digital converter is a mechanism which takes a continuous-time continuous-amplitude signal and converts it to a discrete-time discrete-amplitude signal. The final output of the converter generates a digital signal at the Nyquist rate (twice the bandwidth of interest).

Analog-to-digital converters can be broken down into two categories - Nyquist-rate and oversampled. In Nyquist-rate converters, the analog signal is sampled at the Nyquist rate and converted to digital words. In oversampled converters, the analog signal is sampled at a much higher frequency but the final output of the converter is at the Nyquist rate.

1.1. Nyquist-Rate Analog-to-Digital Converters

Figure 1.1 shows a basic Nyquist-rate converter. The first stage filters the analog signal to a bandwidth acceptable for sampling. The next stage samples this continuous-time signal at the Nyquist rate making a discrete-time analog signal. The last stage converts this discrete-time continuous-amplitude (analog) signal to a discrete-time discrete-amplitude (digital) signal. Usually the majority of the converter is the quantizer.

The purpose of the antialiasing filter is to suppress any signals or noise that is outside the baseband, f_b. This is done so that when sampling is performed these frequency components outside the baseband are not aliased into the baseband. Because the sampling occurs at the Nyquist rate ($2f_b$), any frequency components just outside the baseband are aliased into the baseband. This means the antialiasing filter must be quite

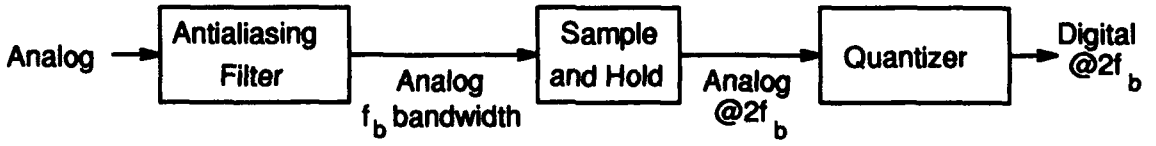


Figure 1.1. Nyquist rate analog to digital converter.

sharp depending on how much bandwidth is to be usable. Typically the middle of the transition band is at the edge of the baseband.

The sample-and-hold circuit is the analog equivalent of a digital D-latch. The circuit operates in two phases like the D-latch. During the sample phase, the output of the circuit tracks the input. During the hold phase, the output stays constant keeping the value that was present at the input at the end of the sample phase. The quantization occurs during the hold phase, because this is the phase when the signal is discrete-time. For quantization circuits which operate in a single cycle, the sample phase can be a significant portion of the total conversion time.

The goal of the quantizer is to convert the held analog value into the closest corresponding digital value. For sufficiently active inputs, quantization is equivalent to the addition of random white quantization noise [1]. The quantizer basically performs a rounding operation. For a n-bit converter, there should be 2^n-1 rounding thresholds. For the quantizer to be linear, the thresholds should be equally spaced.

The time needed for various quantizers may be on the order of 1 to 2^n cycles. Flash quantizers do the conversion in a single cycle by comparing the input to all 2^n-1 in parallel. A problem with this quantizer is that on the order of 2^n matching analog components are needed. It may be difficult to have this many components on one integrated circuit and have all of them matching [2]. Laser trimming may have to be utilized to get accurate resolution.

For successive approximation or algorithmic quantizers, n cycles are needed to make a conversion. These two quantizers break the 2^n-1 thresholds into a binary tree. The quantizer starts at the root threshold to find the most significant bit and continues down the tree until the least significant bit is found. With these quantizers, on the order of 1 or n matching analog components are needed depending of the structure of the quantizer.

In the serial quantizers, 2^n-1 cycles are needed because the input is compared to all thresholds, one threshold at a time. An advantage of the serial quantizer over most of the other quantizers is that a significant amount of matching components are not needed to generate the thresholds.

The ideas from the above quantizers may be combined to form hybrid quantizers. An example would be an algorithmic converter which generates m bits per cycle. To generate the m bits, a flash quantizer can be used.

1.2. Oversampled Analog-to-Digital Converters

Figure 1.2 shows a basic oversampled analog to digital converter. The first stage filters the analog signal to a bandwidth acceptable for sampling. The modulator gener-

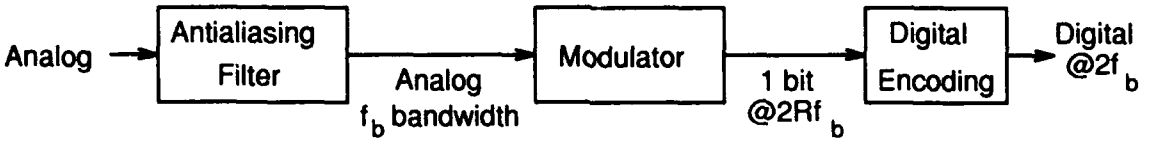


Figure 1.2. Oversampled analog to digital converter.

ates a stream of bits corresponding to the analog signal at R times the Nyquist rate. Some oversampled converters generate more than one bit at the output of the modulator, but most only generate one bit. The last stage encodes the bit stream into n-bit digital words at the Nyquist rate.

The oversampling ratio R is on the order of 2^{an}, where a is less than 1. Higher order modulators have a smaller a. The amplitude resolution increases faster than the time resolution decreases. The conversion time is then better than serial converters and usually not quite as good as successive approximation or algorithmic converters.

Because the modulator samples at a much higher rate than the Nyquist rate, the antialiasing filter does not need to be so sharp. The transition band of the antialiasing filter can extend from f_b to f_s-f_b or $(2R\text{-}1)f_b$. The antialiasing filter can be simply a resistor and capacitor or nothing if there is no significant frequency components beyond the sampling frequency. There is also some aliasing that can occur when final output is decimated down to the Nyquist rate but this can be handled by a digital filter in the digital encoding stage.

Because the sampling frequency is much higher than the baseband, the input changes very little during the a sampling period. Therefore, a sample-and-hold circuit is not needed.

There are two basic types of oversampled modulators - delta and sigma-delta. Both have a similar structure containing a 1-bit quantizer and one or more integrators. They both have similar ideal performance and each model can be converted to the other model with some additional logic [3].

With the delta modulator, the integrator(s) are in the feedback path. The one-bit output of the delta modulator represents the change in the signal from the last sample. A problem with this circuit is slope overload in which the modulator is unable to keep up with the input. Slope overload makes the requirements for antialiasing filter more strict. Another problem with delta modulation is that DC inputs cannot be resolved because the output of the modulator represents the change in the input. Because the output of the modulator represents a change in the input, the digital encoder can be one or more accumulators.

With the sigma-delta modulator, the integrator(s) are in the feedforward path. The average value of the one-bit output of the sigma-delta modulator is approximately the input. If the input to the modulator is positive, then more 1's ($+V_{REF}$ analog) are seen at the output. If the input is negative, then more 0's ($-V_{REF}$ analog) come out. Because the output of the sigma-delta modulator oscillates about the input, a good digital encoder for this modulator is a low-pass filter. Since it is a low-pass filter, it can be used as an antialiasing filter also.

Both of these oversampled modulators are very robust because of the small number of components needed and the large tolerances. Sigma-delta modulation seems to be even more robust than delta modulation because of the position of the integrator [3].

1.3. Testing Analog-to-Digital Converters

Testing can be divided into two categories - static and dynamic. With static tests, various DC analog inputs are tested. One such test could examine each of the analog inputs which lie on a midpoint of a pair of thresholds and check to see whether a correct digital output is obtained.

In a dynamic test, a pure sinusoid within the bandwidth of interest is applied to the converter for many input cycles. Usually the method for assessing the performance of the converter is by finding the signal-to-noise ratio through the use of an FFT algorithm. Two measures can be used to find the number of significant bits in the output - the maximum signal-to-noise ratio and the dynamic range. The maximum signal-to-noise ratio should ideally occur with a full-scale peak-to-peak amplitude, but usually occurs at about 1/2-scale due to overloading. The dynamic range is the ratio of the full-scale amplitude to the amplitude of the input in which the signal-to-noise ratio is 1 (0 dB). Both the maximum signal-to-noise ratio [4] in octaves and the dynamic range in octaves (1 octave = 6.02 dB) can be used to represent the number of bits of resolution.

2. Sigma-Delta Conversion

Figure 2.1 shows a common type of sigma-delta converter which uses a one-bit modulator. The modulator operates in the input format (i.e. analog) and contains a quantizer which quantizes a value in the input format to a single bit. The low-pass filter converts the bit stream from the modulator to the output format (i.e. digital) and does computations in that format.

With this structure, practically any value representation can be converted to any other representation. This is possible because a single bit can easily be interpreted in any format. The modulator and filter can be analog, digital, residue, etc. For analog to digital conversion, the modulator is analog and the filter is digital.

This chapter mainly deals with different modulators. The analysis can be used for any type of value conversion. An ideal low-pass filter is assumed to process the output of the modulator.

2.1. First-Order Sigma-Delta Modulator

A first-order sigma-delta modulator is shown in Figure 2.1. In an implementation there are usually only two major components which make up this model. The first major component is an integrator which usually includes the adder and parts of the gain stages in addition to its accumulating transfer function. The other major component is a quantizer which is modeled by the addition of quantization error and other parts of the gain stages. The main part of the quantizer is a comparator which outputs a bit. Another part of the quantizer converts the bit back to the appropriate format (i.e. 1-bit digital-to-analog converter).

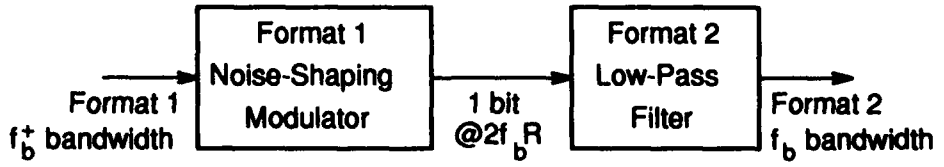


Figure 2.1. Sigma-delta converter with one-bit modulator.

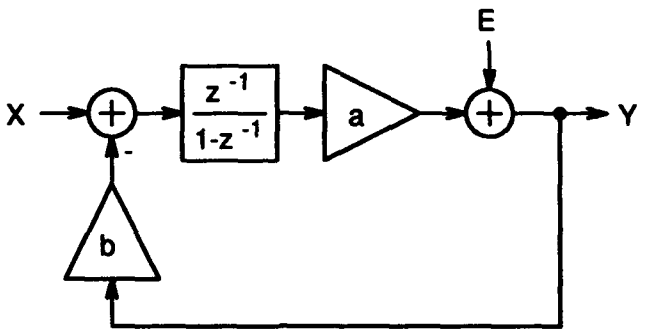


Figure 2.2. First-order sigma-delta modulator.

From Figure 2.2, the output of the modulator is

$$Y = E + a\frac{z^{-1}}{1-z^{-1}}(-bY + X) \tag{2.1}$$

$$Y = \frac{ab}{1+(ab-1)z^{-1}}\left[\frac{1}{b}z^{-1}X + \frac{1}{ab}\left(1-z^{-1}\right)E\right] \tag{2.2}$$

This function has a pole at ab-1, so for the system to be stable, ab should be less than 2. To have no signal attenuation, ab should be 1, making the pole at zero.

With a multi-bit quantizer, its gain is fixed at the ratio of output level spacing to the threshold spacing. This ratio is meaningless for the single threshold quantizer. The quantizer chooses what a should be, compensating for the integrator gain. The gain of the integrator is arbitrary.

Because of the negative feedback, the quantizer tends to help stabilize the system. The following hypothesis will be made about the gain of the quantizer in sigma-delta modulators:

The gain of the single threshold quantizer tends to force the summation of the poles to be at zero.

For this to be true, the coefficient of the z^{-1} term has to be zero because it is equal to the sum of the poles. So, for this coefficient to be zero for the first-order modulator (and for the only pole to be zero),

$$a = \frac{1}{b} \tag{2.3}$$

which makes the output to be

$$Y = \frac{1}{b}z^{-1}X + \left(1-z^{-1}\right)E \tag{2.4}$$

If the modulator is to have a unity gain, b should be 1.

From this function it can be seen that the input passes through with just a linear phase shift and possibly a gain, but the amplitude is not distorted. The quantization noise (assumed to be white) is shaped by a differencing function, though. With low frequencies in the quantization noise, this differencing attenuates the noise. The shaped output noise of the modulator is

$$N = \left(1 - z^{-1}\right)E \tag{2.5}$$

and its frequency response is ($z=e^{j2\pi fT}$)

$$|N| = \left|2\sin(\pi fT)E\right| \approx \left|(2\pi fT)E\right| \tag{2.6}$$

which is a good Taylor series approximation for frequencies in the bandwidth.

Assuming an ideal low-pass filter is used after the modulator, only the frequency components in the bandwidth ($-f_b$ to $+f_b$) of this noise will be part of the final noise. Using Parsevel's relation, the energy in the noise after an ideal low-pass filter is

$$N_B^2\tau = T\int_{-f_B}^{f_B} |N|^2 df \tag{2.7}$$

where τ is the total time over which the energy is measured. The RMS of the noise is *then*

$$N_B \approx \frac{\pi E}{\sqrt{3\tau}} R^{-1.5} \tag{2.8}$$

where R is the oversampling ratio or $(2f_bT)^{-1}$. From this equation, it can be seen that for every doubling of the oversampling ratio, the noise is decreased by $2^{1.5}$ or 1.5 bits are gained for analog-to-digital conversion.

2.2. Second-Order Sigma-Delta Modulator

A second-order sigma-delta modulator is shown in Figure 2.3. The basic addition to the first-order modulator is another integrator. Another second-order structure similar to Figure 2.3 except a delay is not present in the first integrator is analyzed in [5]. The reason the model of Figure 2.3 is used is that the delay makes the integrator easier to implement.

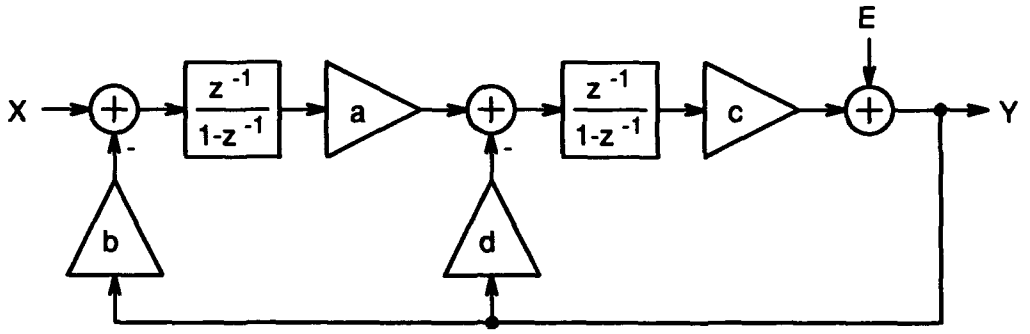


Figure 2.3. Second-order sigma-delta modulator.

From Figure 2.3, the output of the modulator is

$$Y = E + c\frac{z^{-1}}{1-z^{-1}}\left[-dY + a\frac{z^{-1}}{1-z^{-1}}(-bY + X)\right] \tag{2.9}$$

$$Y = \frac{abc}{1+(cd-2)z^{-1}+(1-cd+abc)z^{-2}}\left[\frac{1}{b}z^{-2}X + \frac{1}{abc}\left(1-z^{-1}\right)^2 E\right] \tag{2.10}$$

Using the same hypothesis as above about the gain of the single-threshold quantizer, the quantizer gain is

$$c = \frac{2}{d} \tag{2.11}$$

Defining

$$A \equiv \frac{ab}{d} \tag{2.12}$$

the output is

$$Y = \frac{2A}{1+(2A-1)z^{-2}}\left[\frac{1}{b}z^{-2}X + \frac{1}{2A}\left(1-z^{-1}\right)^2 E\right] \tag{2.13}$$

This function has a pole at $2A$-1, so for the system to be stable, A should be less than 1. If one does a similar analysis on the second-order sigma-delta modulator in [5], the system will be stable if A is less than 2. This result agrees with experimental results in [5], so the hypothesis seems to be true about the gain of the quantizer.

To make both poles of the modulator to be zero, the following must be true

$$A = \frac{1}{2} \tag{2.14}$$

which makes the output to be

$$Y = \frac{1}{b}z^{-2}X + \left(1 - z^{-1}\right)^2 E \tag{2.15}$$

Just as in the first-order modulator, b should be 1 for the modulator to have unity gain.

Although the gain of the first integrator is not arbitrary as in the second integrator and the only integrator in the first-order modulator, the noise and signal levels do not change much with changes in the gain of the first integrator as shown experimentally in [5]. This would not be true if the quantizer had multiple thresholds because the quantizer would not be able to compensate.

Comparing (2.15) to (2.4), one can see the second-order modulator has a noise transfer function which is the square of the noise transfer function of the first-order modulator. This tends to attenuate the noise at low frequencies even more. The RMS noise in the bandwidth is

$$N_B \approx \frac{\pi^2 E}{\sqrt{5}} R^{-2.5} \tag{2.16}$$

With this noise, every doubling of the oversampling ratio will add 2.5 bits of the resolution to the final filtered output for an analog-to-digital converter.

2.3. Multi-Stage Sigma-Delta Modulator

If one extends Figure 2.3 to have 3 loops and 3 integrators, a third-order of noise attenuation can be achieved theoretically. A problem is that the modulator easily goes into unstable states as experimentally studied in [5].

A better way to make high-order modulators is shown in Figure 2.4 [6, 7]. The goal of this structure is to have the second modulator cancel out the quantization error from the first and to shape the noise from the second modulator even more.

In this structure it is assumed that the quantization error can be extracted from the first modulator. This is done by taking a difference across the addition node within the quantizer. For this to be possible, the quantizer gain must be unity. This means the gain of the last integrator is not arbitrary. This combined with the goal of canceling out the quantization error in the first modulator makes component matching much more important than in the previous modulators.

The modulators in Figure 2.4 are of order M_1 and M_2. Either or both of these modulators can even be multi-stage modulators. It is assumed that the higher-order

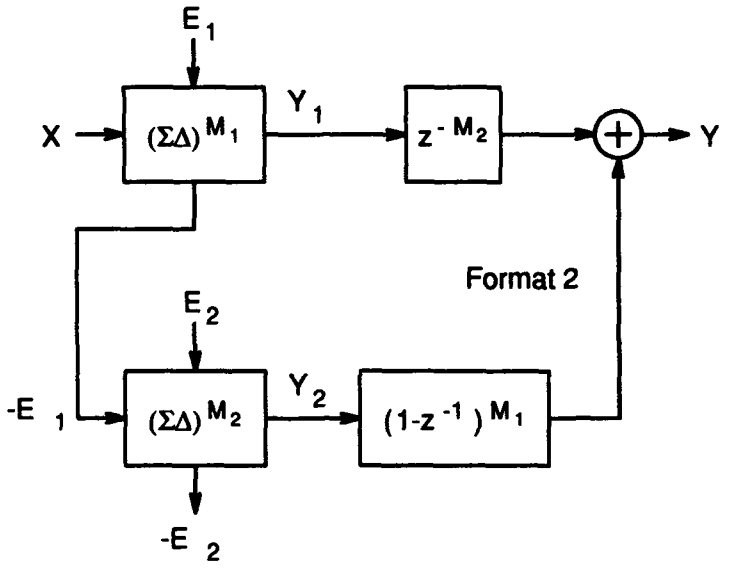


Figure 2.4. Multi-stage sigma-delta modulator.

modulators have an output similar to (2.4) and (2.15) except with the appropriate exponent. With this assumption, the outputs of the two modulators are

$$Y_1 = z^{-M_1}X + \left(1 - z^{-1}\right)^{M_1}E_1 \tag{2.17}$$

$$Y_2 = -z^{-M_2}E_1 + \left(1 - z^{-1}\right)^{M_2}E_2 \tag{2.18}$$

and the output of the whole modulator structure is

$$Y = z^{-M_2}Y_1 + \left(1 - z^{-1}\right)^{M_1}Y_2 \tag{2.19}$$

$$Y = z^{-(M_1+M_2)}X + \left(1 - z^{-1}\right)^{M_1+M_2}E_2 \tag{2.20}$$

From this equation it can be seen that the order of this multi-stage modulator is

$$M = M_1 + M_2 \tag{2.21}$$

The RMS noise of a sigma-delta modulator of order M is

$$N_B \approx \frac{\pi^M E}{\sqrt{(2M+1)\tau}} R^{-\left(M+\frac{1}{2}\right)} \tag{2.22}$$

Every doubling of the oversampling ratio will add M+0.5 bits of resolution to the output of the ideal filter for analog-to-digital conversion. If the modulator is to be used for

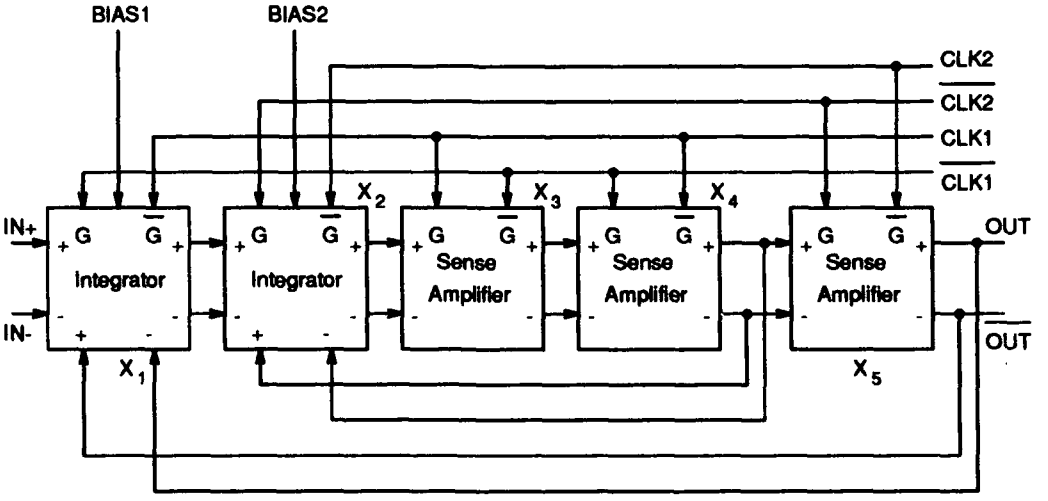
analog-to-digital conversion and the order of the modulator is about equal to the number of bits of resolution, the sigma-delta performance approaches the performance of a pipelined algorithmic analog-to-digital converter.

In the multi-stage structure, it can be observed that the final output of the modulator cannot be represented by just a single bit. If both of the sub-modulators are first-order, the output will be the sum of three bits. Because the filter operates in the output format, the right half of the modulator should also operate in the output format (digital for an analog-to-digital converter).

3. Sigma-Delta Modulator #1

In this project two second-order sigma-delta modulators have been designed. Both of these designs operate with a 512 MHz sampling clock. These designs use GaAs MESFETs with a gate length of 1.2μm. Both modulator designs use buffered-FET logic in the digital portions of the circuits. Both designs use continuous-time integrators with special clocking schemes so that they can be modeled in the discrete-time domain. The first modulator design uses integrators which are based on the square-law of MESFETs. The second modulator design uses integrators which use operational amplifiers.

This chapter discusses the design of the first modulator. A block diagram of the circuit is shown in Figure 3.1. The sub-circuit sizes in the associated table are relative to the minimum sub-circuit sizes defined later. The *A* variable is used on the second integrator to increase the effective gain of the first integrator to 1/2 and still keep its ou-



Element	X1	X2	X3	X4	X5
Size	1 (A=1)	1 (A=8)	1	3	1

Figure 3.1. Sigma-delta modulator.

puts within a linear range. The three sense amplifiers make up a clocked comparator. One-bit digital-to-analog converters are contained within the integrators. Throughout this circuit, differential signals are used.

Since the modulator operates at a much higher frequency than the input, it is assumed that the input to the modulator is approximately constant over each sampling period. During each clock phase, only one integrator is active. Because of this the inputs of the integrators are constant during each clock period. This allows the modulator to be modeled after Figure 2.3 which has discrete-time integrators. This clocking scheme allows the integrators not to be sensitive to the delay of sense amplifiers. In [8], it is experimentally shown how the shaping of the quantization noise changes for a first-order modulator as the quantizer delay is changed.

This sigma-delta modulator uses three power supplies for the analog parts of the circuit and three power supplies for the digital parts. The analog portions of the modulator use a sourcing +10V supply, a sinking -4V supply, and ground. The digital portions of the modulator use a sourcing +6V supply, a sinking -1V supply, and a +2V supply. The modulator accommodates an analog input signal in the range -0.6V to +0.6V.

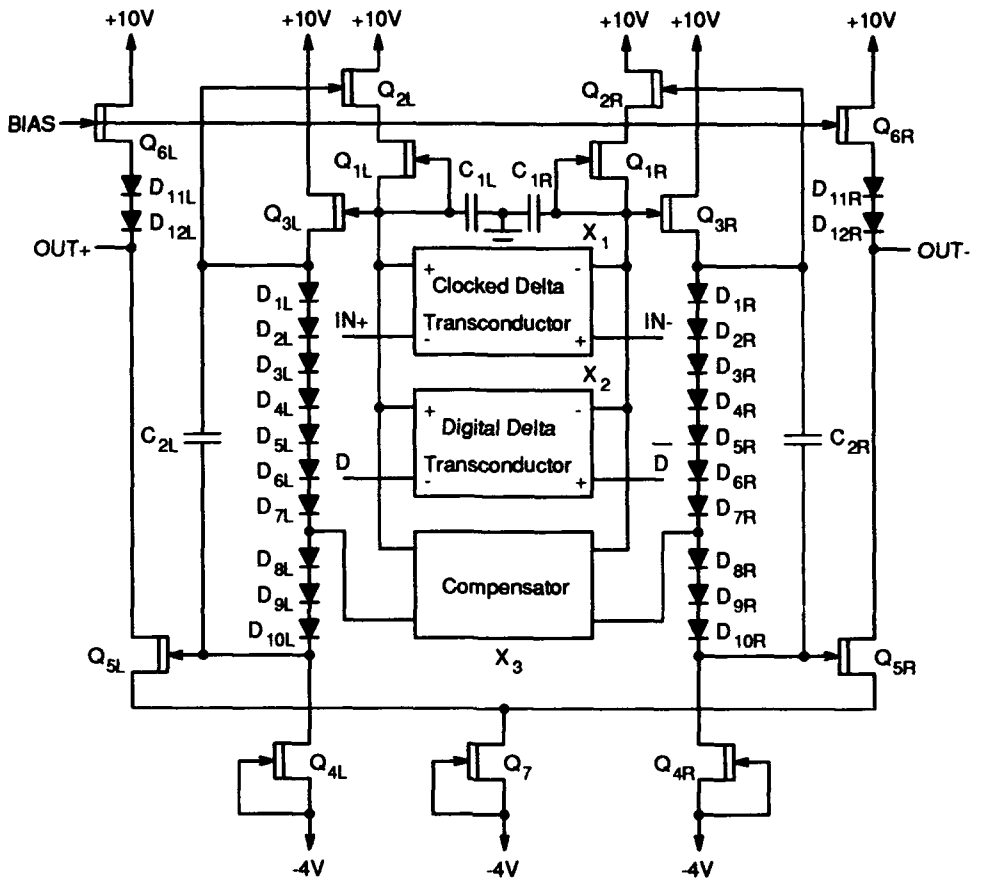
3.1. Integrator

The integrator circuit is shown in Figure 3.2. The transistor and diode sizes shown in the table are relative to the minimum size (1.2μm by 1.2μm). The *A* variable allows the analog input to have a higher gain than the digital input. The integrator has two main stages plus a level-shifting stage in the middle. The first stage is the integrating stage which uses the square law of FETs to accomplish the integration. The last stage is an output stage used to remove any common mode variations.

Figure 3.3 shows a simulation of both integrators. In this simulation, the input is zero. The integrating current for the first integrator corresponds to either the positive or negative reference voltage. The integrating current for the second integrator corresponds to the same reference voltage plus the output of the first integrator. This figure shows the two integrators operating in two different non-overlapping phases.

3.1.1. Integrating stage

A model of the integrating stage is shown in Figure 3.4. Each dependent current source corresponds to each of the transistors Q_1 and Q_2 and circuit X_3 of Figure 3.2. Each of the transistors Q_1 and Q_2 of Figure 3.4 corresponds to the circuits X_1 and X_2 of Figure 3.2. To keep the transistors on and the gates reverse-biased, the input range is allowed to be from -0.6V to +0.6V.



Element	X3	X4	X5	Q1	Q2	Q3	Q4	Q5	Q6	Q7	D1-D10
Size	A	1	A+1	2(A+1)	16(A+1)	8	1	4	1	2	1

Element	C1	C2
Size	3.7p	0.4p

Figure 3.2. Integrator.

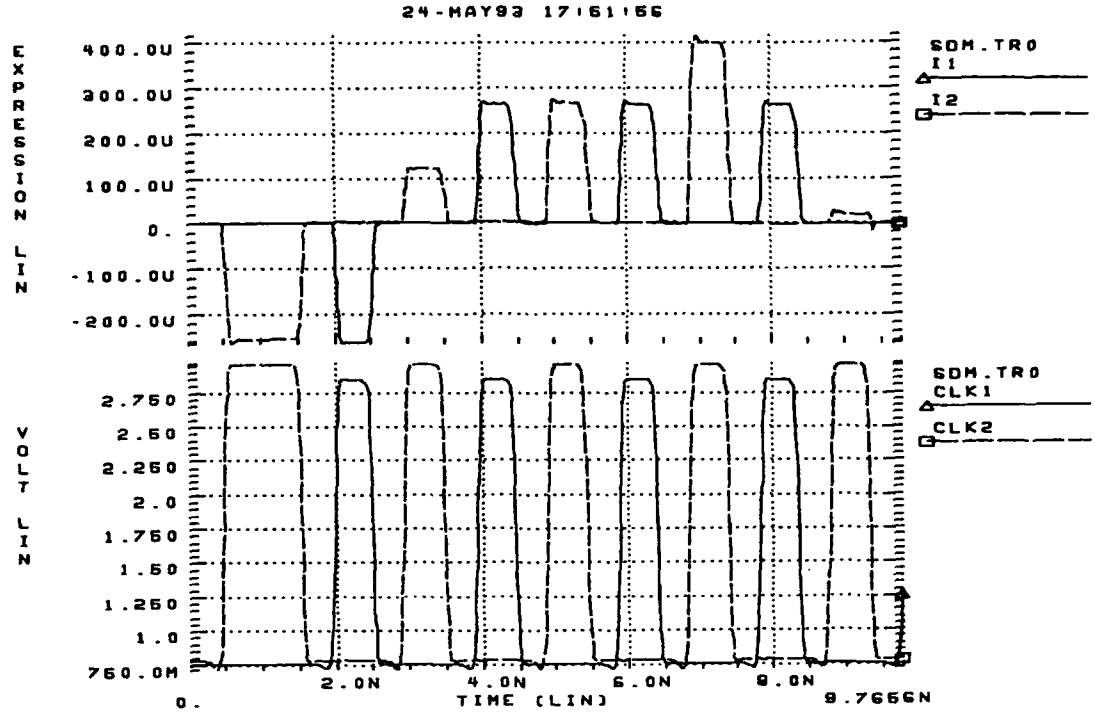


Figure 3.3. Currents through the integrating capacitors of the both integrators.

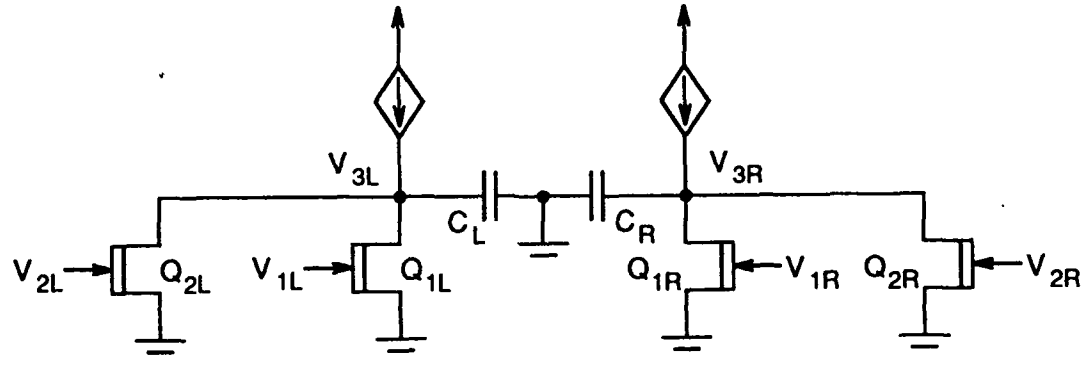


Figure 3.4. Integrating stage of the integrator.

To achieve the best output resistance, each Q_1 of Figure 3.2 is kept in saturation which means the voltage across it should be at least a threshold voltage of the MESFET. To achieve this, each Q_3 is used to shift up by half of the threshold and each Q_2 is used for the other half. Using the square-law for FETs, the ratios of Q_3 to Q_4 and Q_2 to Q_1 should be 4 to have half-threshold shifts. To account for any other non-linearities (output resistance, backgating), these ratios are made to be 8 which makes the voltage across each Q_1 even greater.

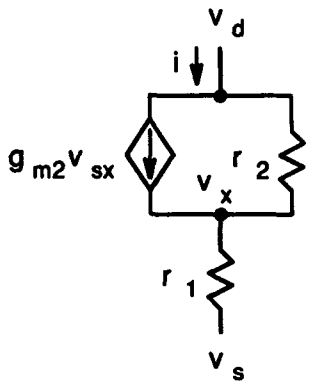


Figure 3.5. Model of the high impedance current source.

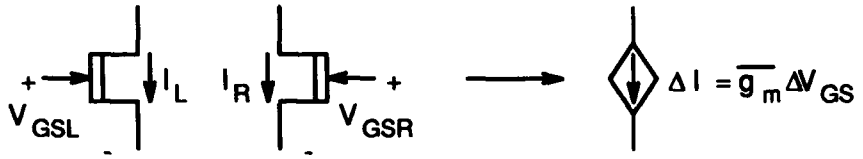


Figure 3.6. Delta transconductor transformation.

A model of a current source is shown in Figure 3.5. With this model, it is assumed that each Q_3 and each Q_4 form a perfect voltage follower. The system of equations for this model is

$$\begin{bmatrix} \frac{1}{r_2} & -g_{m2}-\frac{1}{r_2} \\ -\frac{1}{r_2} & g_{m2}+\frac{1}{r_2}+\frac{1}{r_1} \end{bmatrix} \begin{bmatrix} v_{ds} \\ v_{xs} \end{bmatrix} = \begin{bmatrix} i \\ 0 \end{bmatrix} \tag{3.1}$$

Solving this using Kramer's rule, the output resistance is

$$\frac{v_{ds}}{i} \approx g_{m2}r_2r_1 \tag{3.2}$$

To analyze Figure 3.4, each pair of transistors will be transformed into what will be a *delta transconductor*. This transformation is shown in Figure 3.6 and is valid for large signals.

If one neglects velocity saturation effects and output resistance, the current through each transistor is

$$I = \beta\left(V_{GS}-V_T\right)^2 = \beta\left[\left(\overline{V_{GS}}-V_T\right)^2 \pm \left(\overline{V_{GS}}-V_T\right)\Delta V_{GS} + \left(\frac{\Delta V_{GS}}{2}\right)^2\right] \tag{3.3}$$

and its transconductance is

$$g_m \equiv \frac{\partial I}{\partial V_{GS}} = 2\beta\left(V_{GS} - V_T\right) \tag{3.4}$$

When the current difference is taken, the result is

$$\Delta I = 2\beta\left(\overline{V_{GS}} - V_T\right)\Delta V_{GS} = \overline{g_m}\Delta V_{GS} \tag{3.5}$$

This result says that when the common-mode element of the input is constant, the delta transconductance is constant. When this occurs, the delta transconductor can be used for large signals. Figure 3.7 shows the variances of the transconductances of the transistors and the delta transconductance. This simulation includes all of the non-linearities as modeled by HSPICE.

When the delta transconductor model is used with Figure 3.4 and a similar process is performed for the capacitors, the model of Figure 3.8 is found. In this model R is the net output resistance of the current sources and the transistors forming the delta transconductances. This resistance should be sufficiently high. It cannot be argued that the delta output resistance of the integrating transistors is linear, but the delta output resistance of the current sources is linear and dominates R in the implementation. From Figure 3.8, the output of the integrating stage is

$$\Delta V_3 = -\left(\frac{\overline{g_{m1}}}{C}\right)\frac{\Delta V_1}{s+\frac{1}{RC}} - \left(\frac{\overline{g_{m2}}}{C}\right)\frac{\Delta V_2}{s+\frac{1}{RC}} \approx -\left(\frac{\overline{g_{m1}}}{C}\right)\frac{\Delta V_1}{s} - \left(\frac{\overline{g_{m2}}}{C}\right)\frac{\Delta V_2}{s} \tag{3.6}$$

The previous analysis only examines the output difference. To keep outputs within range, the dependent current sinks of Figure 3.9 are used. This circuit causes negative feedback to help stabilize the outputs.

To increase the output resistance of these compensating current sinks, each Q_4 and each X are used to keep the drain of the each Q_3 almost constant. The middle power supply of each buffered-FET inverter X is +2V, so the drain of each Q_3 is approximately +2V which will always keep each Q_3 in saturation.

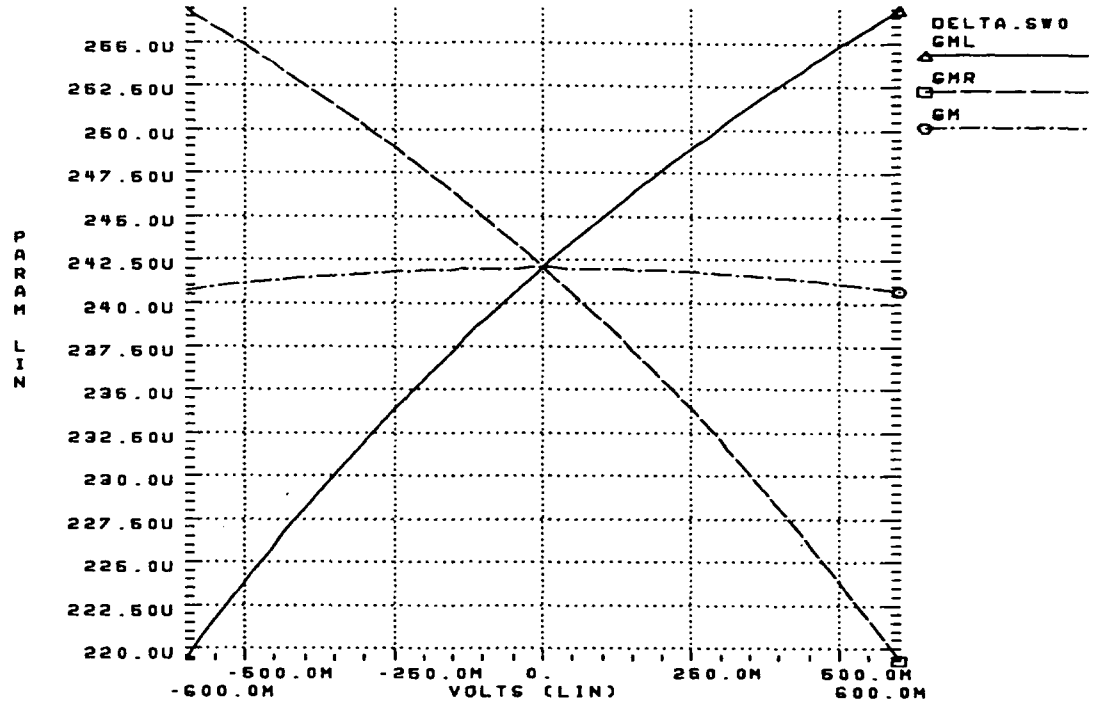


Figure 3.7. Simulated transconductances and delta transconductance.

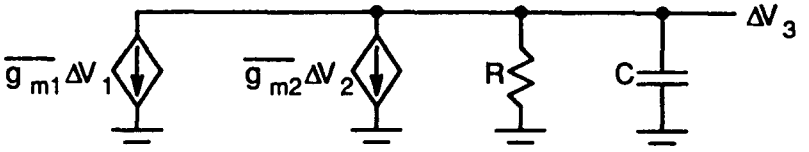
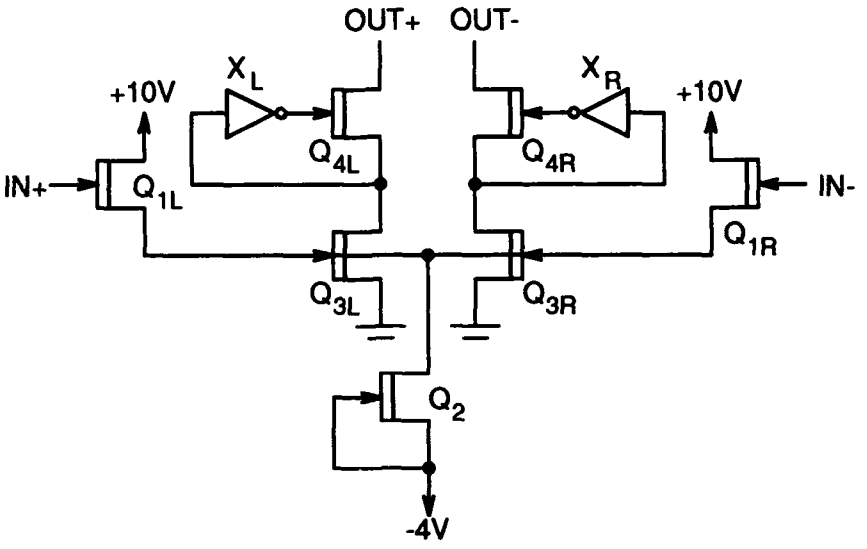


Figure 3.8. Delta model of the first stage of the integrator.



Element	X	Q1	Q2	Q3	Q4
Size	1	1	2	1	4

Figure 3.9. Compensator.

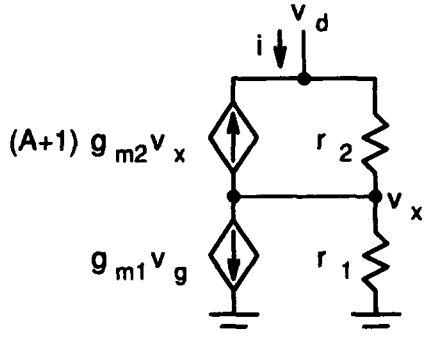


Figure 3.10. Regulated sinking transistor.

The model of one of these current sinks is shown in Figure 3.10. Assuming the gain of an inverter is -*A*, the system of equations for this model is

$$\begin{bmatrix} \frac{1}{r_2} & -(A+1)g_{m2} - \frac{1}{r_2} \\ -\frac{1}{r_2} & (A+1)g_{m2} + \frac{1}{r_2} + \frac{1}{r_1} \end{bmatrix} \begin{bmatrix} v_d \\ v_x \end{bmatrix} = \begin{bmatrix} i \\ g_{m1} v_g \end{bmatrix} \tag{3.7}$$

so the output resistance is

$$\left. \frac{v_d}{i} \right|_{v_g=0} \approx (A+1) g_{m2} r_2 r_1 \tag{3.8}$$

which is an order higher than the output resistance of the current sources of the integrator.

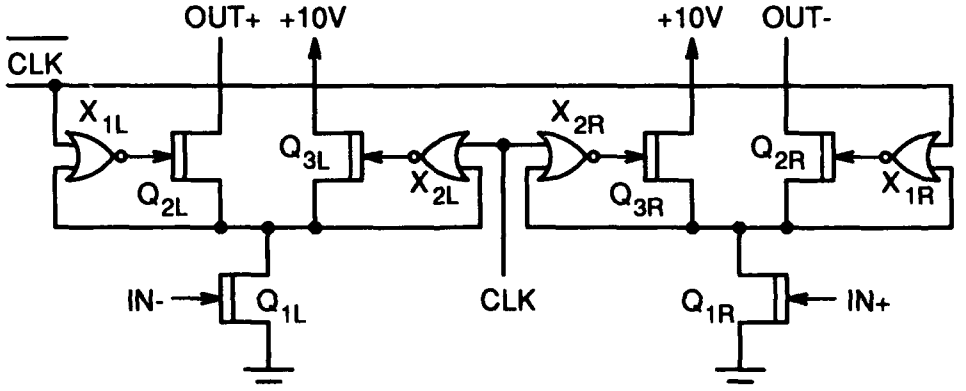
The clocked delta transconductor is shown in Figure 3.11. It is the basic transistor pair in the delta transconductor except that the currents from these transistors are switched. This circuit is used for the analog input to the integrator. In this circuit, buffered-FET NOR gates are used.

When the clock is high (and the integrator is active), each X_2 output will be low and each Q_3 will be off. Each X_1 acts as a an inverter so during this phase, each half of the circuit can be modeled by Figure 3.10 making the output resistance (3.8).

An advantage to having an inverter help improve the output resistance is that the drain of each Q_1 does not vary much, even when the input changes. This allows the square law to hold more closely than with a simple cascode circuit.

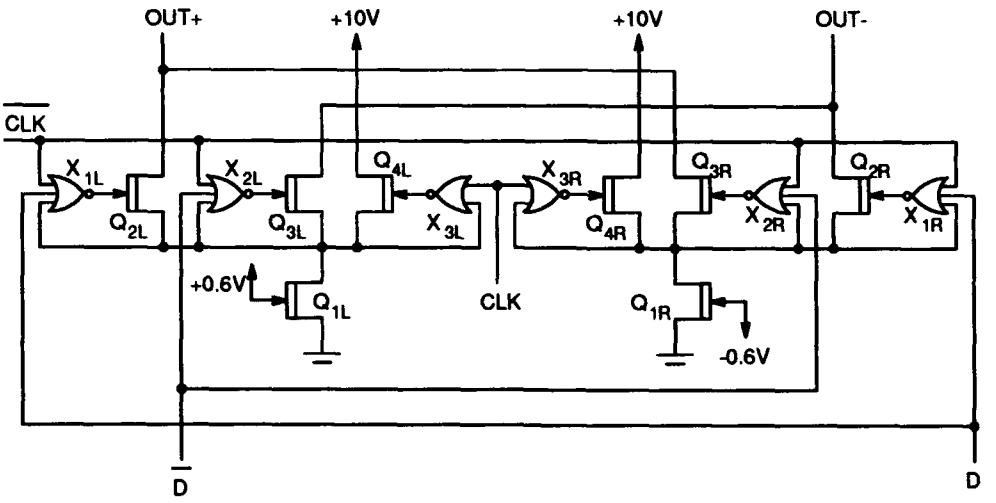
When the clock is low (and the integrator is inactive), the current will be switched through a dummy path. This technique is similar to the one used in the switched current source in [9]. The dummy path is used so that the drain of each Q_1 does not have to be charged and discharged during each phase. This also causes less capacitive feedthrough to the analog inputs.

The digital delta transconductor is shown in Figure 3.12. It is equivalent to a one-bit digital-to-analog converter (DAC) and a clocked delta transconductance. When the clock is high, the digital inputs control whether the positive and negative reference voltages are used in the left and right branches or vice-versa. When the clock is low the currents are routed through dummy paths.



Element	X1	X2	Q1	Q2	Q3
Size	1	1	1	4	4

Figure 3.11. Clocked delta transconductor.



Element	X1	X2	X3	Q1	Q2	Q3	Q4
Size	1	1	1	1	4	4	4

Figure 3.12. Digital delta transconductor

3.1.2. Output Stage

One purpose of the last stage of the integrator is to bias the output at a level compatible with the next circuit. The output of the first integrator goes to the second integrator so its output should be biased at 0 V. The BIAS voltage for the first integrator was about 1.6V. The output of the second integrator goes to a digital-like sense amplifier which should have inputs about 2 V. The BIAS voltage for the second integrator was about 1.8V.

Another purpose of the output stage is to increase the gain of the integrator. Using some symmetry arguments, the differential model of one half of the output stage is shown in Figure 3.13. This circuit can be described by the equation

$$v_{out}\left(g_{m6}+\frac{1}{r_5}+\frac{1}{r_6}\right) = -g_{m5}v_{in}+i \tag{3.9}$$

so the differential gain of the circuit is

$$\left.\frac{v_{out}}{v_{in}}\right|_{i=0} \approx -\frac{g_{m5}}{g_{m6}} = -\sqrt{\frac{W_5}{W_6}} \tag{3.10}$$

and the output resistance is

$$\left.\frac{v_{out}}{i}\right|_{v_{in}=0} \approx \frac{1}{g_{m6}} \tag{3.11}$$

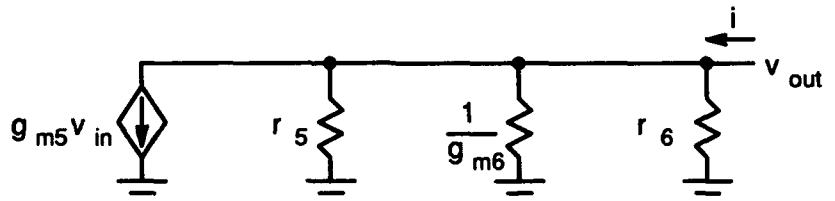


Figure 3.13. Differential model of one half of the output stage of the integrator.

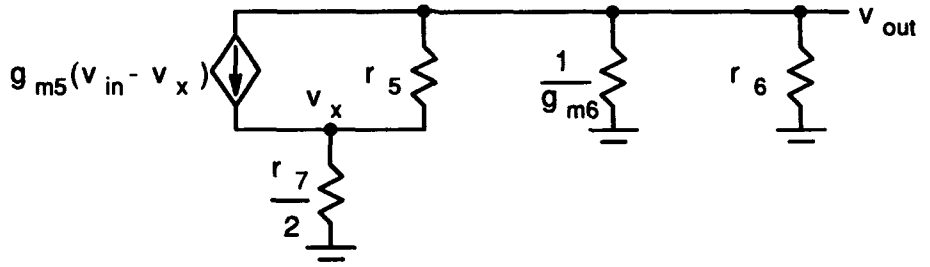


Figure 3.14. Common mode model of one half of the output stage of the integrator.

A final purpose of the last stage of the integrator is to remove any common-mode variations. The common-mode variations need to be removed for the first integrator because its outputs go to the second integrator. According to (3.5), the common-mode input voltage needs to be constant for the delta transconductance to be linear. Using some more symmetry arguments, the common-mode model of one half of the output stage is shown in Figure 3.14. The system of equations that describe this model is

$$\begin{bmatrix} g_{m6} + \frac{1}{r_5} + \frac{1}{r_6} & -g_{m5} - \frac{1}{r_5} \\ -\frac{1}{r_5} & g_{m5} + \frac{1}{r_5} + \frac{2}{r_7} \end{bmatrix} \begin{bmatrix} v_{out} \\ v_x \end{bmatrix} = \begin{bmatrix} -g_{m5}v_{in} \\ g_{m5}v_{in} \end{bmatrix} \tag{3.12}$$

making the common-mode gain to be

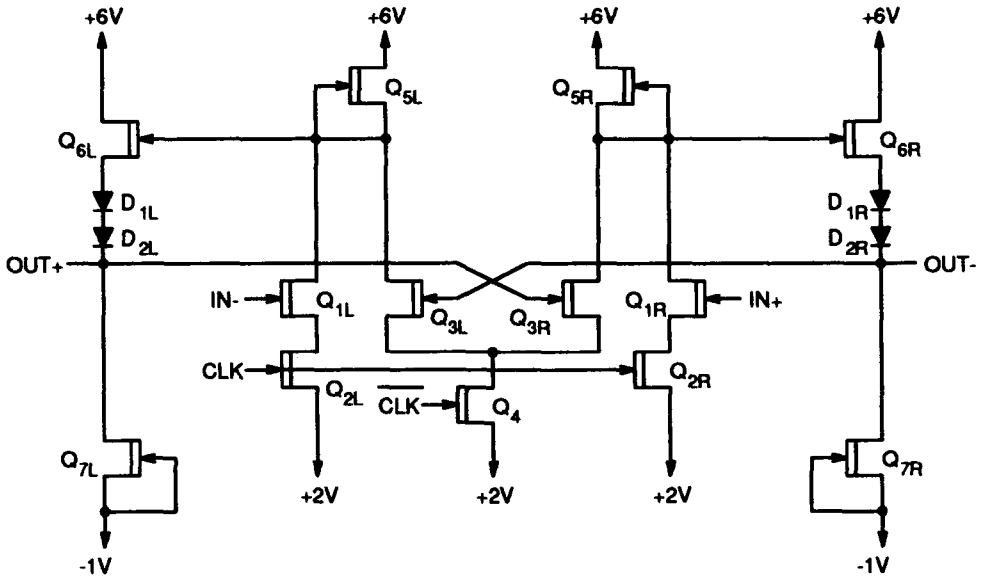
$$\frac{v_{out}}{v_{in}} \approx -\frac{2}{g_{m6}r_7} \tag{3.13}$$

which has an absolute value much smaller than 1.

3.2. Sense Amplifier

The sense amplifier is shown in Figure 3.15. This circuit operates in two phases - sample and sense.

During the sample phase (when the clock is high), the sense amplifier just becomes a pair of inverting amplifiers. Assuming the source follower stage of the circuit is ideal, a model of one of these inverting amplifiers is shown in Figure 3.16. The sys-



Element	Q1	Q2	Q3	Q4	Q5	Q6	Q7	D1-D2
Size	1	8	1	16	1	1	1	1

Figure 3.15. Sense amplifier.

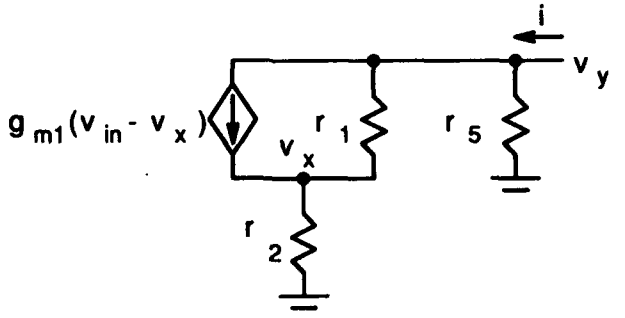


Figure 3.16. Model of one half of the sense amplifier during the sampling phase.

tem of equations for this model is

$$\begin{bmatrix} \frac{1}{r_1}+\frac{1}{r_5} & -g_{m1}-\frac{1}{r_1} \\ -\frac{1}{r_1} & g_{m1}+\frac{1}{r_1}+\frac{1}{r_2} \end{bmatrix} \begin{bmatrix} v_y \\ v_x \end{bmatrix} = \begin{bmatrix} i-g_{m1}v_{in} \\ g_{m1}v_{in} \end{bmatrix} \tag{3.14}$$

so the gain is

$$\left.\frac{v_y}{v_{in}}\right|_{i=0} \approx -g_{m1}\left(r_1 \parallel r_5\right) \tag{3.15}$$

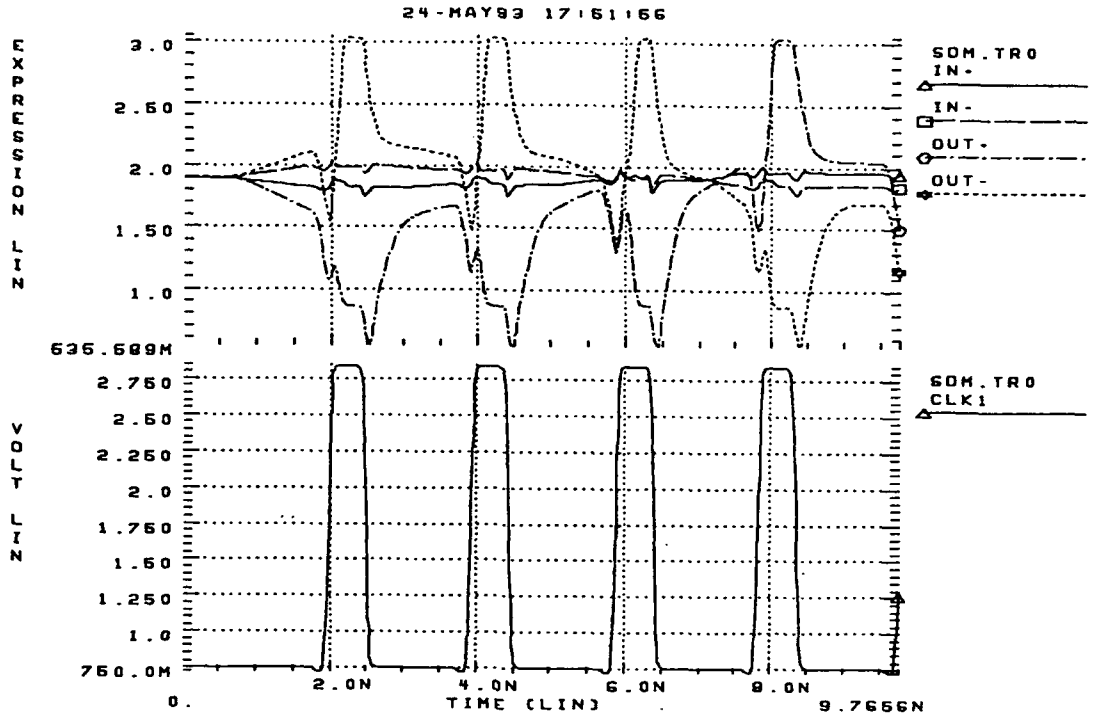


Figure 3.17. Simulation of the sense amplifier.

This approximation assumes that the r_2 is quite small because Q_2 is large and in the triode region. The output resistance before the level shifting stage is

$$\left.\frac{v_y}{i}\right|_{v_{in}=0} \approx r_1 \parallel r_5 \tag{3.16}$$

During the sense phase (when the clock is low), the sense amplifier acts as a flip-flop. The sign of the output difference before the sense phase determines what state the flip-flop will rush to. The positive feedback causes the magnitude of the output difference to be increased until a stable state is reached. Figure 3.17 shows a simulation of the sense amplifier showing both the sample and sense phases.

3.3. Simulation

The whole circuit was simulated by the HSPICE [10] software using MESFET models from the Vitesse 1.2μm process. The models included most of the nonlinearities including backgating. Backgating was neglected on the current sources in the integrators, because it severely degraded the performance. It was assumed that these current sources could be isolated or a special buffer layer as in [11] could be used in fabrication.

Two primary simulations were done to analyze the performance of the sigma-delta modulators. In both of these simulations, a pure sinusoidal 4 MHz input was used over 32+ cycles or 4096+ samples. Both of these simulations took about 6 days to complete.

The first simulation done used an input with an amplitude of half of the full-scale (full-scale amplitude is 0.6V). This simulation was done to find the approximate maximum signal-to-noise ratio. Overloading causes the signal-to-noise ratio to decrease if a higher amplitude input was used [5,12,13,14].

The second simulation done used an input with an amplitude of 1/128 of the full-scale. This simulation was done to find the approximate dynamic range using the fact that for small inputs, the signal to noise ratio will be proportional to the amplitude of the input.

The output of the modulator was analyzed using the PV-WAVE [15] software. To get a frequency spectrum of the modulator output, the output was first multiplied by a Hanning window and then a FFT was performed. The windowing did cause some frequency smearing, but gave results that were much less dependent upon the number of samples taken. Figure 3.18 shows the frequency spectrum of the output of the sigma-delta modulator for the two HSPICE simulations.

In observing these frequency spectrums, it can be seen that no major harmonic distortion is present. This tends to indicate that the nonlinearities in using the square-law of FETs for integration did not significantly degrade performance. In the frequency spectrum it is observed that the noise flattens out at a corner frequency somewhere between 1/64 and 1/32 of the sampling rate. With ideal integrators, the noise would continue decreasing at the same rate. From the frequency spectrums, it can be concluded that the real integrators have s-poles somewhere between -1/64 and -1/32 of the sampling rate. These non-zero s-poles are due to the finite output resistances of the current supplies.

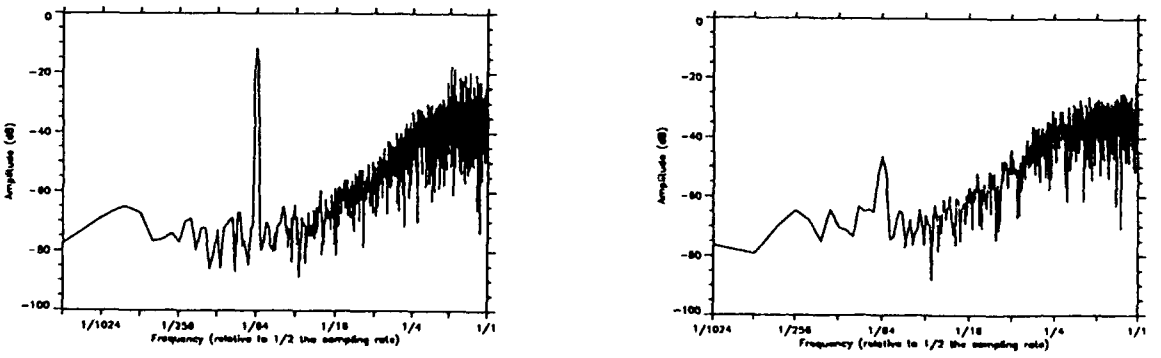


Figure 3.18. Frequency spectrums of 1/2-scale and 1/128-scale 4 MHz inputs.

Table 3.1. Resolution for 4 MHz inputs.

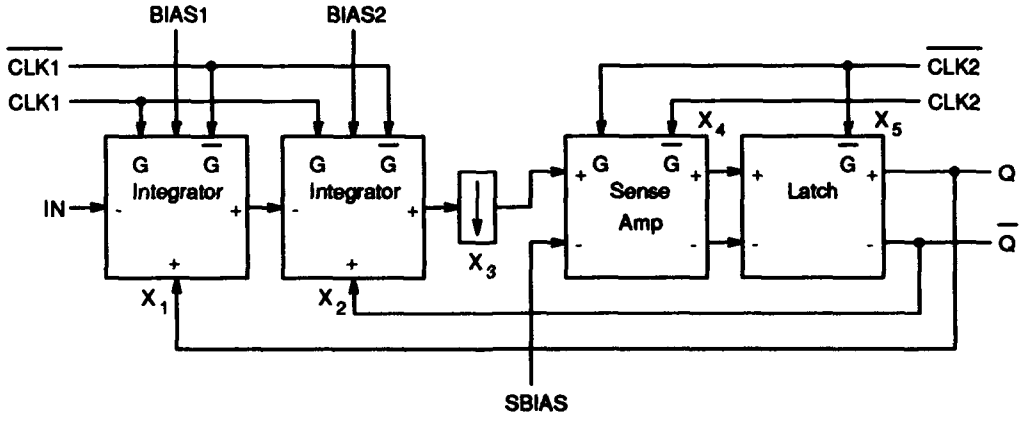
Oversampling ratio	Signal to noise plus distortion (1/2-scale)	Signal to noise plus distortion (1/128-scale)	Estimated dynamic range (1/128-scale)
64	205 (7.7 bits)	3.47	444 (8.8 bits)
32	136 (7.1 bits)	2.67	342 (8.4 bits)
16	70.8 (6.1 bits)	1.36	174 (7.4 bits)

When calculating the signal to noise plus distortion ratio, an ideal filter was assumed. Parsevel's relation was used to calculate the RMS of the signal and of the noise. To handle frequency smearing, frequency components around the peak frequency component which were much greater than the noise were used as part of the signal. Table 3.1 shows the results of the signal to noise plus distortion calculations and the estimated dynamic ranges. These results seem to indicate that an oversampling ratio of 32 seems to be a good trade-off.

4. Sigma-Delta Modulator #2

The main differences between this design and the previous design have to do with the integrators. The primary change is that the integrators use op-amps instead of the square law of the transistors. Another difference is that the integrators use single-ended signals instead of differential ones. A third difference is that the integrators are inverting. Because the integrators are inverting, the first integrator receives the positive output and the second integrator receives the negative output. A final difference is that only the digital inputs to the integrators are clocked. Like the previous design the circuit is clocked at 512 MHz and a 4 MHz input signal was used.

All of the signals before the level shifter are analog and are in the range from -1V to +1V. Unlike the previous design, the range was not limited by gate to source voltage of the transistors. The analog range is now limited by the how much level shifting is done and how large the power supply voltages are. The signals after the level



Element	X1	X2	X3	X4	X5
Size	1 (A=1)	1 (A=7/3)	1	2	1

Figure 4.1. Sigma-delta modulator.

shifter are mostly digital and are in the range -4V to -2V. Level shifting is needed between the second integrator and the sense amplifier because the input range of the sense amplifier is not in the output range of the integrator.

Excluding ground and the reference voltages, only three main power supplies are needed. A +6V supply is used in the analog circuits and is used for sourcing current. For the digital circuits, ground is used to source current. A -3V supply is used in the analog circuits for generating biased current sinks. In the digital circuits, the -3V supply is connected to the switching transistors. A -5V supply is used in the analog circuits to create current sinks so that the current sinks connected to the -3V supply can be controlled. The -5V supply is used in the digital circuits for level shifting.

Like the previous modulator design, the digital inputs are clocked into the integrator to make the modulator insensitive to the quantizer delay. The analog inputs are not clocked into the integrator, though. Because of this, the integrator can not be modeled as a simple discrete-time accumulator.

The modified model of the second-order sigma-delta modulator is shown in Figure 4.2 which takes into account the characteristics of the integrators. In the first integrator, the analog input is assumed to be approximately constant over each sampling period because the modulator oversamples the input. Because of this, the first integrator is modeled as a discrete-time accumulator. The analog input to the second integrator changes linearly over each period because it comes from the first integrator. To model this linear function for the second integrator, the average of the current and previous samples of the first integrator is taken as the analog input.

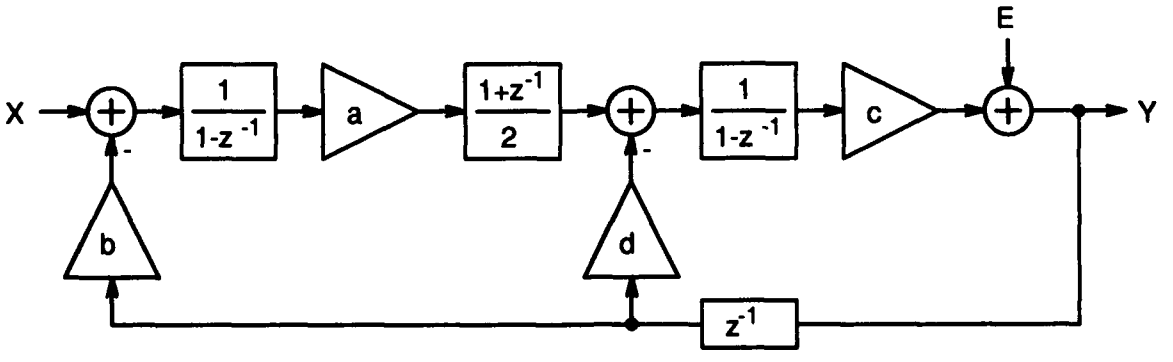


Figure 4.2. Model of the sigma-delta modulator.

From Figure 4.2, the output of the modulator is

$$Y = E + c\frac{1}{1-z^{-1}}\left[-dz^{-1}Y + a\left(\frac{1+z^{-1}}{2}\right)\left(\frac{1}{1-z^{-1}}\right)\left(-bz^{-1}Y + X\right)\right] \tag{4.1}$$

$$Y = \frac{abc}{1+\left(cd-2+\frac{abc}{2}\right)z^{-1}+\left(1-cd+\frac{abc}{2}\right)z^{-2}}\left[\frac{1}{b}\left(\frac{1+z^{-1}}{2}\right)X + \left(1-z^{-1}\right)^2 E\right] \tag{4.2}$$

Using the same as (2.3) and (2.11),

$$c = \frac{2}{d+\frac{ab}{2}} \tag{4.3}$$

Defining

$$A \equiv \frac{ab}{d} \tag{4.4}$$

the output will be

$$Y = \frac{4A}{2+A+\left(3A-2\right)z^{-2}}\left[\frac{1}{b}\left(\frac{1+z^{-1}}{2}\right)X + \left(1-z^{-1}\right)^2 E\right] \tag{4.5}$$

To get rid of the transfer function on the left part of the this expression,

$$A = \frac{2}{3} \tag{4.6}$$

which makes the output

$$Y = \frac{1}{b}\left(\frac{1+z^{-1}}{2}\right)X + \left(1-z^{-1}\right)^2 E \tag{4.7}$$

To allow this function to have unity gain at DC b should be 1. Unlike the second-order modulator in Figure 2.3, this modulator attenuates the input signal by a function which takes the average of two samples. Since the modulator oversamples the input though, this averaging will cause very little attenuation. This attenuation function causes this modulator not to be able to be used in a multi-stage modulator, though.

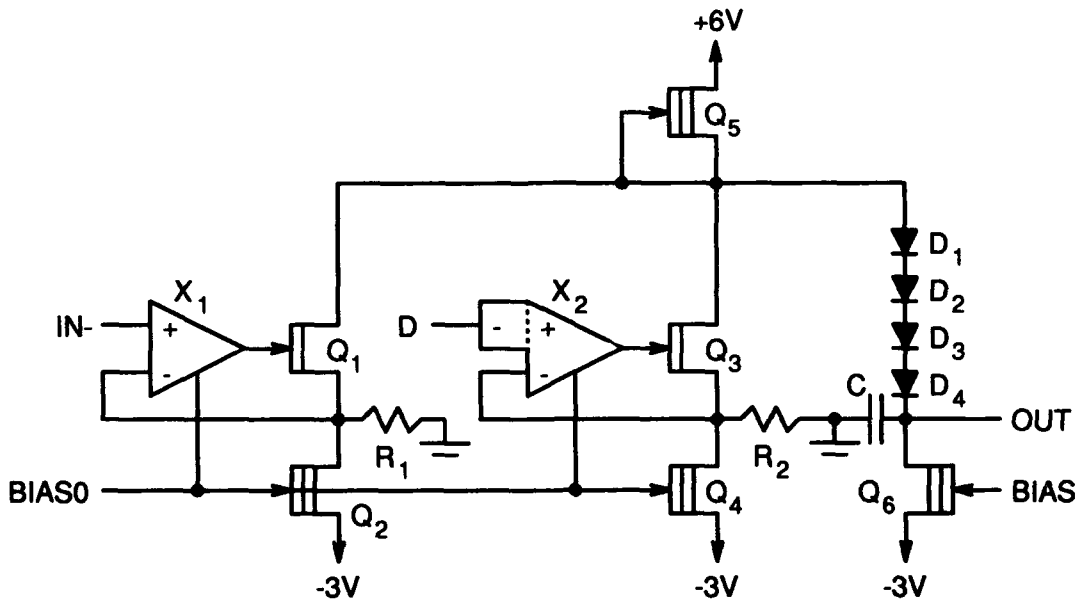
4.1. Integrator

The integrator used is based on the integrator used in [9]. One advantage of this integrator is that the load at the input of the integrator is just a small gate capacitor. For a standard RC integrator, the load at the input is resistive. For a switched-capacitor integrator, the load at the input is a larger capacitor. The reason the input load is taken into consideration is that there are two integrators and the first integrator drives the second.

Another advantage of this integrator is that the op-amp only has to drive a small gate capacitor. Even when other standard integrators are unloaded, the op-amp has to drive the larger integrating capacitor. Because of this configuration, the op-amp can have just one stage.

The integrator is shown in Figure 4.3. The analog input is routed through a normal op-amp and the digital input is routed through a clocked "digital op-amp". The digital op-amp is equivalent to normal op-amp with its non-inverting input connected to a clocked DAC. When the clock is low, the effective non-inverting input is 0V. When the clock is high and the inverting digital input is high, the effective non-inverting input is -1V ($-V_{REF}$). When the clock is high and the inverting digital input is low, the effective non-inverting input is +1V ($+V_{REF}$). Figure 4.4 shows a simulation of the integrator with an analog input of zero. The treatment of the digital input can be seen from this figure.

The sinking transistors are biased so that the total sinking current is equal to the sourcing current. The sum of the currents through the resistors becomes the current through the capacitor, because all of the other currents cancel out. The current through each resistor is proportional to the voltage across that resistor and the voltage across the capacitor will be proportional to the integral of the the current through the capacitor.



Element	X1	X2	Q1	Q2	Q3	Q4	Q5	Q6	D1-D4	R1	R2	C
Size	1	1	1	1	1	1	3	1	1	100k	(54k)A	68f

Figure 4.3. Integrator.

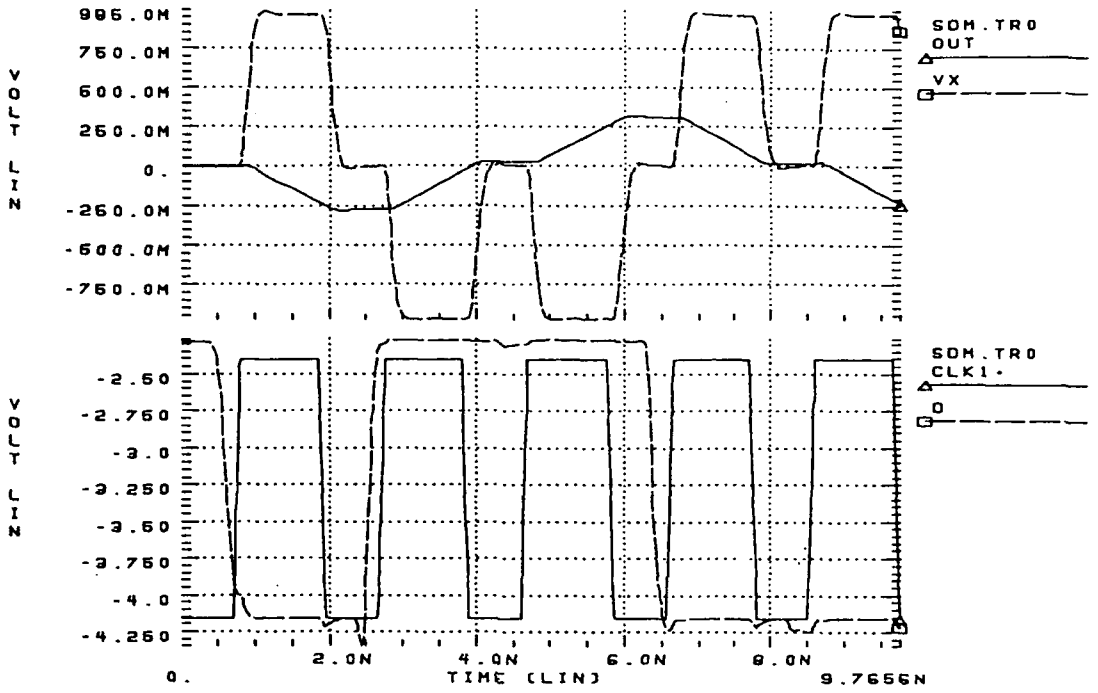


Figure 4.4. Simulation of the integrator.

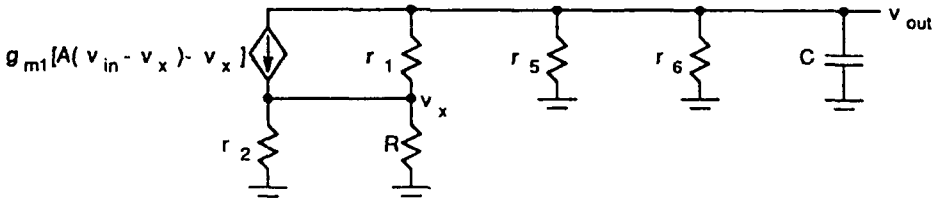


Figure 4.5. Model of the integrator.

The negative feedback with the op-amps causes the voltages across the resistors to be equal to the effective non-inverting inputs of the op-amps. The output will be proportional to the integral of the sum of the effective non-inverting inputs of the op-amps.

The model of the integrator with a single input is shown in Figure 4.4. The analysis for two inputs is similar. From this model, the system of equations is

$$\begin{bmatrix} sC + \frac{1}{r_1} + \frac{1}{r_5} + \frac{1}{r_6} & -(A+1)g_{m1} - \frac{1}{r_1} \\ -\frac{1}{r_1} & (A+1)g_{m1} + \frac{1}{R} + \frac{1}{r_1} + \frac{1}{r_2} \end{bmatrix} \begin{bmatrix} v_{out} \\ v_x \end{bmatrix} = \begin{bmatrix} -g_{m1}Av_{in} \\ g_{m1}Av_{in} \end{bmatrix} \quad (4.8)$$

and the transfer function is

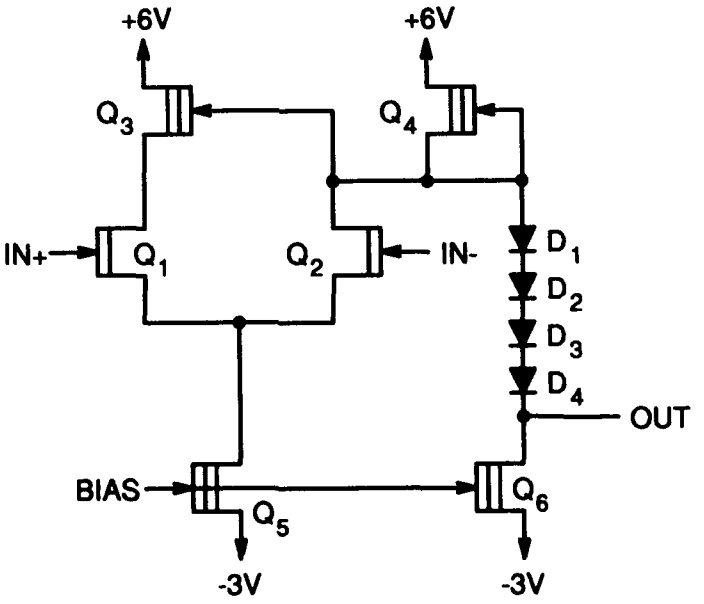
$$\frac{v_{out}}{v_{in}} \approx -\left(\frac{A}{A+1}\right)\frac{1}{(R \parallel r_2)C}\left(s + \frac{1}{(r_5 \parallel r_6)C}\right)^{-1} \approx -\frac{1}{sRC} \tag{4.9}$$

This result shows that the pole of the integrator is mainly not determined by the gain of the op-amp like other integrators, but is determined by the output resistance of the current source. The ideal response is the same as a standard RC integrator.

4.1.1. Operational Amplifier

The operational amplifier designed is similar to the ones in [11,13] except that no output stage is used. Because the load of the operational amplifier is just a small capacitor, a single stage op-amp is used. Because only a single stage op-amp was used, no major frequency compensation was needed.

The operational amplifier is shown in Figure 4.6. The bias voltage is approximately -3V. At the bias point, the current from the left sinking transistor is split equally among the differential pair. The bias gate to source voltage is about zero for the differential transistors. The current from the sourcing transistor on the right is split equally among the right differential transistor and the level shifting diodes.



Element	Q1	Q2	Q3	Q4	Q5	Q6	D1-D4
Size	1	1	1	2	2	1	1

Figure 4.6. Operational amplifier.

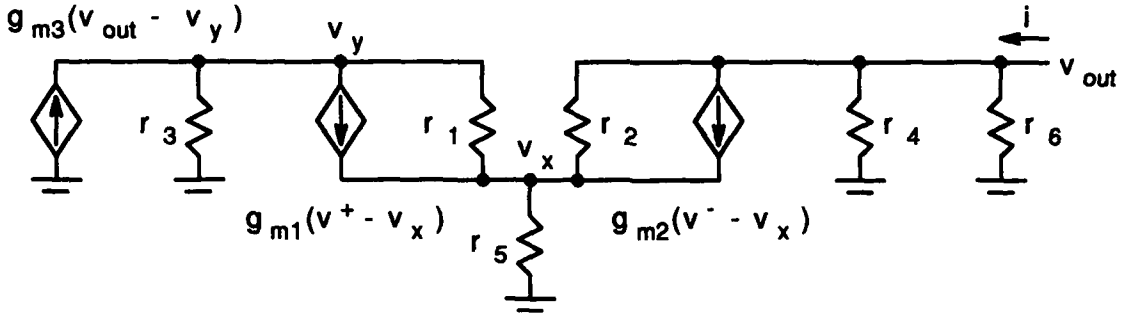


Figure 4.7. Model of the operational amplifier.

The source follower on the left causes the drain to source voltages across the differential transistors to be approximately equal. The difference in the drain voltages will be approximately equal to the differential input. The majority of the output resistance will be due to the sourcing transistor on the right and the sinking transistor on the right.

A model of the operational amplifier is shown in Figure 4.7. In this model the AC resistance of the diodes is neglected. From this model, the system of equations is

$$\begin{bmatrix} \frac{1}{r_2}+\frac{1}{r_4}+\frac{1}{r_6} & 0 & -g_{m2}-\frac{1}{r_2} \\ -g_{m3} & g_{m3}+\frac{1}{r_1}+\frac{1}{r_3} & -g_{m1}-\frac{1}{r_1} \\ -\frac{1}{r_2} & -\frac{1}{r_1} & g_{m1}+g_{m2}+\frac{1}{r_1}+\frac{1}{r_2}+\frac{1}{r_5} \end{bmatrix} \begin{bmatrix} v_{out} \\ v_y \\ v_x \end{bmatrix} = \begin{bmatrix} i-g_{m2}v^- \\ -g_{m1}v^+ \\ g_{m1}v^+ + g_{m2}v^- \end{bmatrix} \quad (4.10)$$

In the following analysis, the fact that Q_1 and Q_2 are sized the same is used. Also, Q_3 must have an output resistance at least on the order of the output resistance of Q_4. The differential gain of the operational amplifier is

$$\left.\frac{v_{out}}{v_{in}}\right|_{i=0,v_{in}=2v^+=-2v^-} \approx \frac{1}{2}g_{m1}\left(r_4 \parallel r_6\right) \quad (4.11)$$

which is not dependent upon the output resistance of the differential transistors due to the source follower Q_3. The common mode gain is

$$\left.\frac{v_{out}}{v_{in}}\right|_{i=0,v_{in}=v^+=v^-} \approx \frac{r_4 \parallel r_6}{2r_5} \quad (4.12)$$

which is about a third for the given transistor ratios. The output resistance is

$$\left.\frac{v_{out}}{i}\right|_{v^+=v^-=0} \approx r_4 \parallel r_6 \quad (4.13)$$

These results show that all transistors except Q_1 and Q_2 need to have a maximum output resistance to achieve the best results.

Figures 4.8 and 4.9 show the simulated results of the operational amplifier. These simulations use op-amps that are only self-loaded because it is known that the output load is very small. It is found that the gain-bandwidth is 400 MHz and the phase margin is 98 degrees. The differential DC gain was 50 and the common-mode gain was 0.3. The offset with the bias circuit shown later was 3.4 mV.

4.1.2. Digital Operational Amplifier

The digital operational amplifier is shown in Figure 4.10. It is basically a normal op-amp with three non-inverting inputs with digital logic to control these three inputs. This method is used instead of a clocked DAC and a normal op-amp because GaAs p-channel transistors are not available, making it difficult to have a good DAC.

During the operation of the circuit only one of the three transistors Q_1, Q_2, and Q_3 are on at a time. The effective non-inverting input is the voltage at the gate of this transistor that is on. The gate of Q_1 switches between the positive reference voltage (+1V) and digital low (about -2.5V). The gate of Q_2 switches between zero and digital low. The gate of Q_3 always stays at the negative reference voltage (-1V).

When the gate of Q_1 is +1V, the common source rises to about +1V because the bias gate to source voltage is about zero. Q_2 and Q_3 turn off because their gates are at least a threshold below the common source. When the gate of Q_1 is digital low, and the gate of Q_2 is zero, the common source will rise to about zero and Q_1 and Q_3 turn off. When the gate of Q_1 and Q_2 are digital low, the right transistor will turn on and Q_1 and Q_2 are off.

When the clock is low, only Q_2 turns on and its gate becomes zero. In the integrator, this means when the clock is low, the digital branch causes no any integration. When the clock goes high, either Q_1 or Q_3 turns on, depending on what the input digital data is. The logic in this circuit made it so that there is no spikes in the output due to delays from the clock to its inverse. This is made possible because of Q_{12} which makes the gate of Q_2 zero when the gate of Q_1 is +1V. When the gate of Q_1 turns off, the effective positive input will fall to the next highest voltage, which is zero.

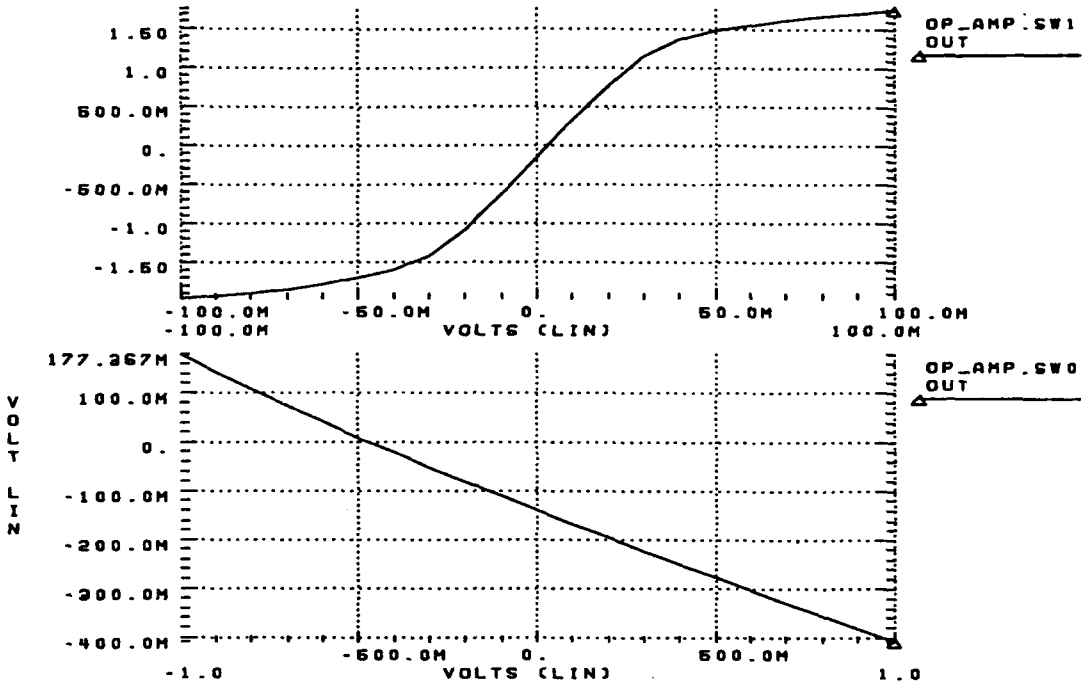


Figure 4.8. Differential and common mode DC analysis of the op-amp.

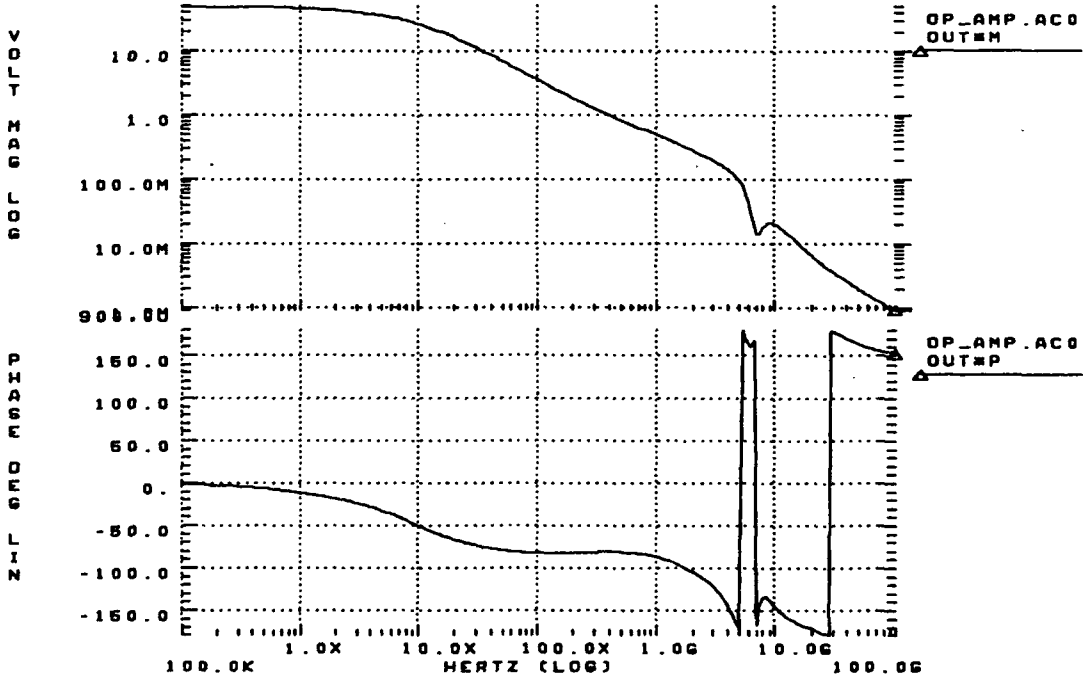
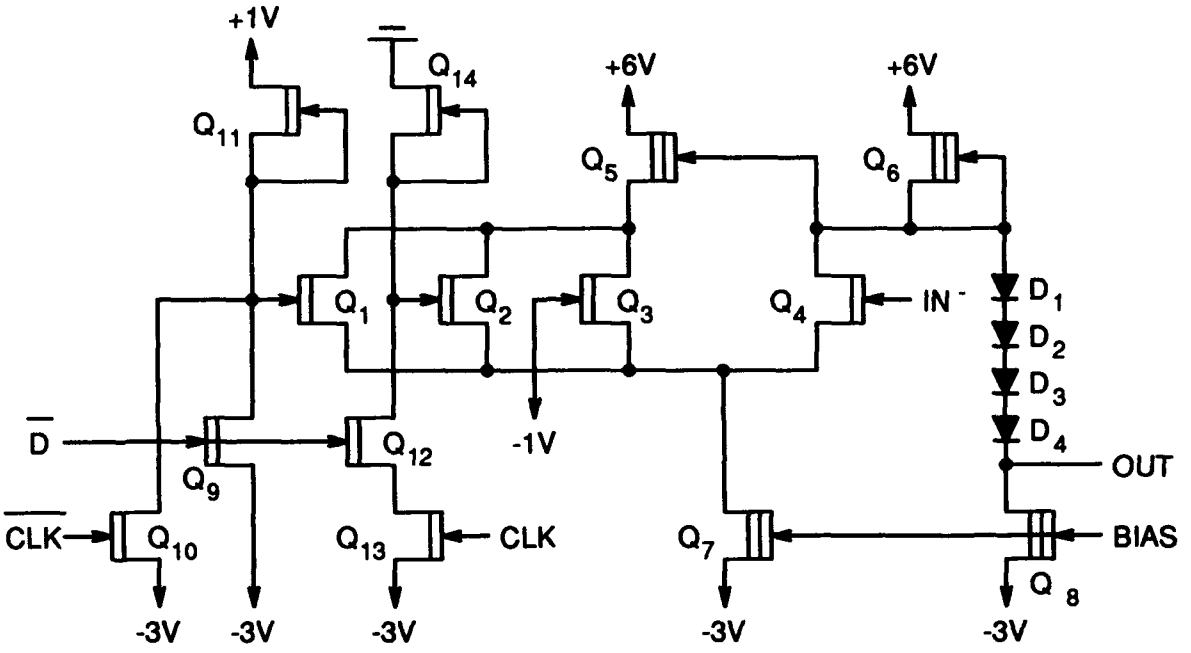


Figure 4.9. AC response of the operational amplifier.



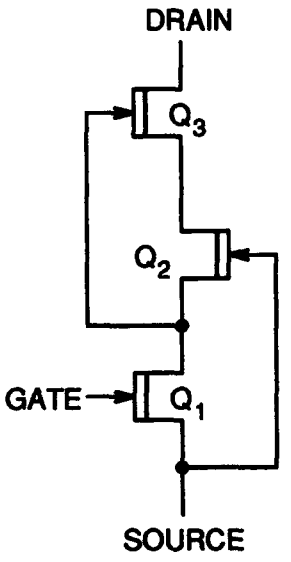
Element	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Size	1	1	1	1	1	1	2	2

Element	Q9	Q10	Q11	Q12	Q13	Q14	D1-D4
Size	2	2	1	2	1	4	1

Figure 4.10. Digital operational amplifier.

4.1.3. Super MESFET

In the some of the figures above a different symbol is used for some of the transistors. For these "super MESFETs", the self-bootstrapped circuit [16] of Figure 4.11 is used instead of a single transistor. In this circuit, Q_2 and Q_3 stay in saturation and their gate to source voltages are about half of the threshold. Assuming the gate to source voltage of Q_1 is about zero, the gate to drain voltage of Q_1 is about half of the threshold. This transistor will operate close to saturation or in saturation because of early saturation effects, so it will have a sufficiently high output resistance. The output resistance of this circuit is one to two orders higher than a simple transistor.



Element	Q1	Q2	Q3
Size	1	4	4

Figure 4.11. Super MESFET.

A model of the super MESFET is shown in Figure 4.12. The system of equations for this model is

$$\begin{bmatrix} \frac{1}{r_3} & -g_{m3}-\frac{1}{r_3} & g_{m3} \\ -\frac{1}{r_3} & g_{m3}+\frac{1}{r_2}+\frac{1}{r_3} & -g_{m2}-g_{m3}-\frac{1}{r_2} \\ 0 & -\frac{1}{r_2} & g_{m2}+\frac{1}{r_1}+\frac{1}{r_2} \end{bmatrix} \begin{bmatrix} v_{ds} \\ v_{ys} \\ v_{xs} \end{bmatrix} = \begin{bmatrix} i \\ 0 \\ g_{m1}v_{gs} \end{bmatrix} \tag{4.14}$$

The output resistance is therefore

$$\left.\frac{v_{ds}}{i}\right|_{v_{gs}=0} \approx g_{m3}r_3 g_{m2}r_2 r_1 \tag{4.15}$$

This resistance is not as high as it may seem because Q_1 is close to saturation but probably not quite in saturation. This means r_1 is not quite as high as r_2 or r_3.

4.2. Sense Amplifier

The sense amplifier is shown in Figure 4.13. It operates in two phases - sampling and sensing. This sense amplifier is similar to the previous design except that some negative feedback transistors are incorporated.

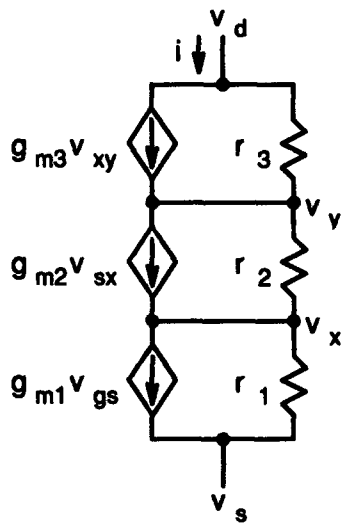
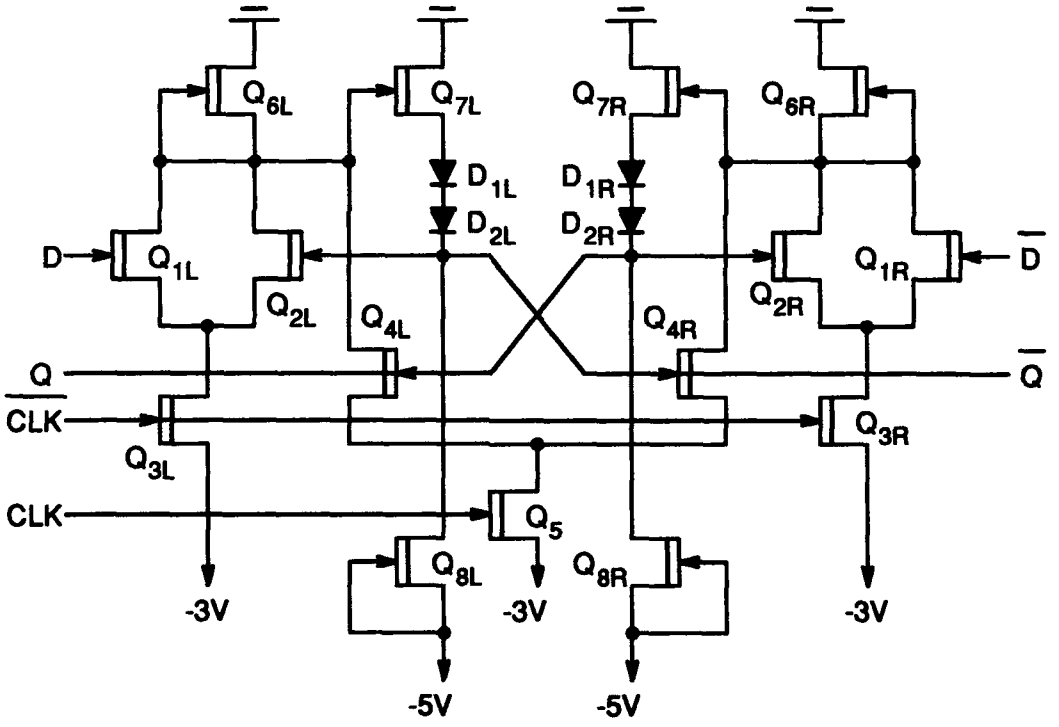


Figure 4.12. Model of the super MESFET.



Element	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	D1-D2
Size	2	2	8	4	16	2	2	2	2

Figure 4.13. Sense amplifier.

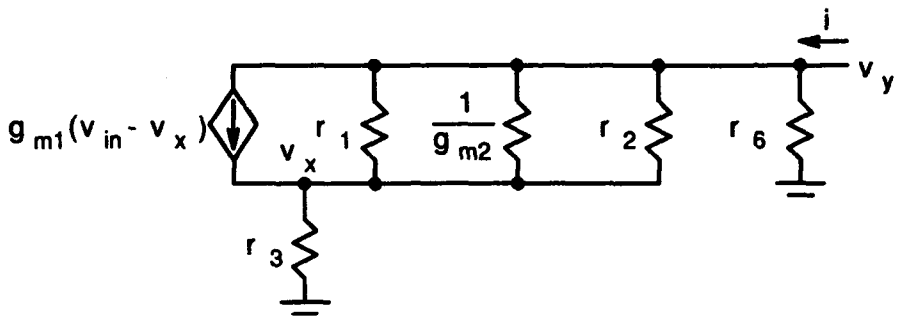


Figure 4.14. Model of half of the sense amplifier during the sampling phase.

During the sample phase, the sense amplifiers act as a pair of low gain (a little less than 1) inverters. The low gain occurs because of the negative feedback transistors (each Q_2) which are turned on along with the sampling transistors (each Q_1) during the sampling phase. One advantage of this low gain is that the input capacitance is reduced because the Miller effect becomes negligible. The other advantage is that the negative feedback causes the output resistance to be tremendously reduced. This causes sampling to be much faster.

A model of the sense amplifier during the sampling phase is shown in Figure 4.14. This model assumes the source follower stage is ideal. The system of equations for this model is

$$\begin{bmatrix} g_{m2} + \frac{1}{r_1} + \frac{1}{r_2} + \frac{1}{r_6} & -g_{m1} - g_{m2} - \frac{1}{r_1} - \frac{1}{r_2} \\ -g_{m2} - \frac{1}{r_1} - \frac{1}{r_2} & g_{m1} + g_{m2} + \frac{1}{r_1} + \frac{1}{r_2} + \frac{1}{r_3} \end{bmatrix} \begin{bmatrix} v_y \\ v_x \end{bmatrix} = \begin{bmatrix} i - g_{m1} v_{in} \\ g_{m1} v_{in} \end{bmatrix} \quad (4.16)$$

The gain of the

$$\left.\frac{v_y}{v_{in}}\right|_{i=0} \approx -\frac{g_{m1}}{g_{m2}} \quad (4.17)$$

which is about 1 for the transistor ratios shown in Figure 4.13. The output resistance before the source follower is

$$\left.\frac{v_y}{i}\right|_{v_{in}=0} \approx -\frac{1}{g_{m2}} \quad (4.18)$$

which is significantly smaller than the resistance of the sense amplifier of the previous modulator design.

During the sense phase, the sampling and negative feedback transistors are turned off and the positive feedback (each Q_4) transistors are turned on. The sense amplifier becomes a pair of cross-coupled inverters and they rush to a stable state. The

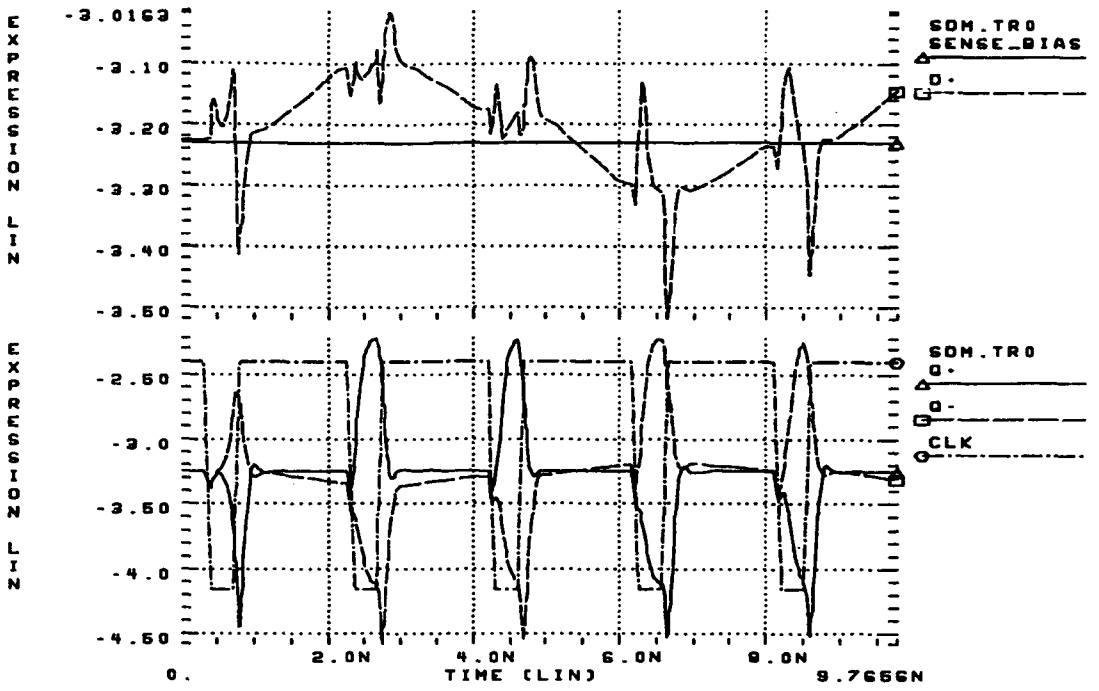
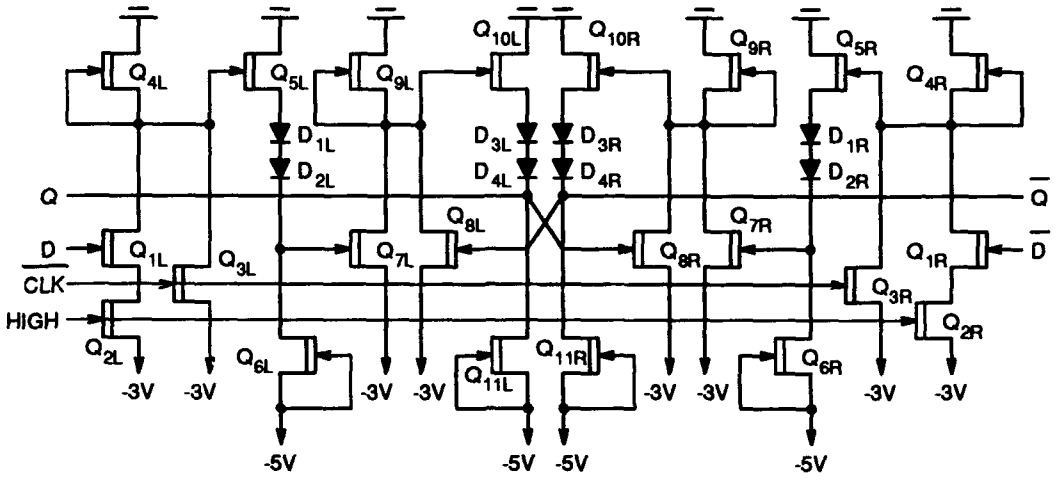


Figure 4.15. Simulation of the sense amplifier.

action of the sense amplifier during this phase is the same as the sense amplifier of the previous modulator design. Figure 4.15 shows a simulation of the sense amplifier.

4.3. Latch

The D-latch is shown in Figure 4.16. In the center is a pair of cross-coupled NOR gates forming a S-R latch. Driving the S and R nodes is another pair of NOR gates so that the S and R nodes are low when the clock is low. A cross-coupled pair of AND-OR-INVERT gates were not used instead of this configuration because the sense amplifiers would exhibit more hyteresis. The NOR gates driving the S and R nodes act as buffers between the sense amplifier and the latch. Each of the Q_2 transistors with their gates always at digital high are used to make the latch react quicker to the sense amplifier. The input stage to the latch is made to match the sense amplifier by adding each transistor Q_2.



Element	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	D1-D2	D3-D4
Size	2	4	2	1	1	1	2	2	1	1	1	1	1

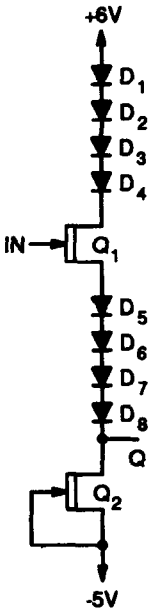
Figure 4.16. Latch.

4.4. Bias Level Shifter

This circuit shown in Figure 4.17 is used to shift voltages in the range -1 - +1 to the range -4 - -2. This means a shift of about 3V and about 4 diodes are needed. The extra 4 diodes connected to +6V are used so that the level shift had less dependence upon the output resistance of the transistors.

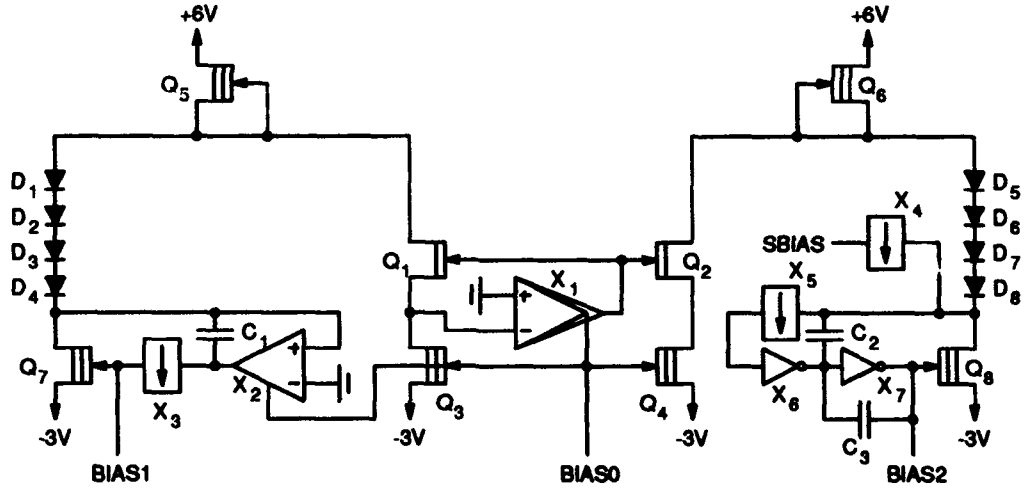
4.5. Biasing Circuit

This biasing circuit shown in Figure 4.18 creates 4 bias voltages. BIAS0 is used by op-amps and the first stage of the integrators so that the offset voltage across the resistors in the integrators is very close to zero. The "super op-amp" is used to accomplish this task. The BIAS1 voltage is made such that the DC output of the first integrator with zero input is approximately zero. The BIAS2 voltage is made such that the DC input to the sense amplifier is a high gain voltage for the sense amplifier. The SBIAS voltage is what the sense amplifier compares to. To get the best SBIAS voltage, the inverters X_6 and X_7 are made to match the sense amplifier much like the input stage to the latch is made. All of these bias voltages were close to 3V.



Element	Q1	Q2	D1-D4	D5-D8
Size	1	1	1	1

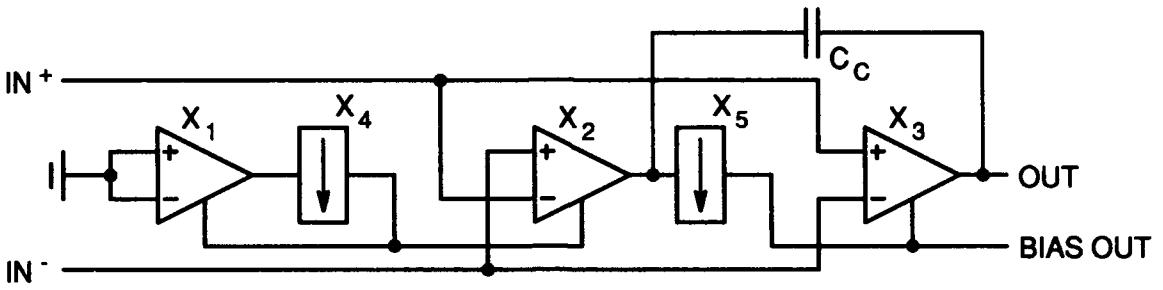
Figure 4.17. Bias level shifter.



Element	X1	X2	X3	X4	X5	X6	X7	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Size	18	4	4	1	1	4	16	32	2	32	2	48	3	16	1

Element	D1-D4	D5-D8	C1	C2	C3
Size	16	1	0.1p	0.4p	0.1p

Figure 4.18. Biasing circuit.



Element	X1	X2	X3	X4	X5
Size	1	1	4	1	4

Figure 4.19. Super operational amplifier.

The super operational amplifier is shown in Figure 4.19. It is basically a two stage op-amp with each stage being a simpler op-amp. Because increasing the bias voltage of a simple op-amp decreases its output, the bias voltage is an inverting input.

The op-amp X_1 on the left is used to bias the op-amp X_2. X_2 is the differential stage which drives the bias voltage of the op-amp X_3. The differential inputs to X_3 do not provide much of the gain because their effect is overwhelmed by the changes in the bias voltage. X_1 looks like all of the other op-amps and its bias voltage should be used so the the offset voltage is as small as possible.

4.6. Simulation

To make the circuit simulate faster, parts of the modulator were replaced by approximate models. The first replacement was for the whole bias circuit. Since the bias voltages stayed fairly constant, the bias circuit was modeled as 4 voltage sources having voltages equal to the DC output simulated for the bias circuit.

Another model used was for the super MESFETs. They were modeled with the effective transconductance, output resistance, bias current, and some capacitors. The optimization features of HSPICE were used to make the best fit for DC and AC characteristics.

The last model used was for each set of level shifting diodes. The model used had a level shifting voltage source, level shifting resistor, and a capacitor. Again the optimization features of HSPICE were used to do the modeling.

The simulation speed compared to the previous modulator circuit was 8.5 faster. This was due to the modeling and to the difference in the circuits.

Because the simulation was faster than than the previous design, simulations with 4 times as many samples as before were done. These simulations took over 16k samples. Each simulation took about 3 days. With the previous design it would have taken a month.

The first simulation that was done with a 4 MHz half-scale (full-scale amplitude is 1.0V) sinusoidal input like used in the previous modulator design. A 2 MHz half-scale input was also simulated for comparison and to test higher oversampling ratios. These two simulations were used to find the maximum signal-to-noise-plus-distortion ratio. The last simulation done used a 2 MHz 1/128-scale input. This input was used for calculating the dynamic range of the sigma-delta modulator.

Using PV-WAVE, the frequency spectrums are shown in Figures 4.20 and 4.21. In these figures it can be seen that there is a DC component. This DC component is present because the digital op-amp is unable to allow the positive and negative reference voltages to have exactly equal times for integrating. This DC component could be taken out by adjusting the reference voltages.

From Figures 4.20 and 4.21 it can be seen that no major harmonic distortion exists and hence the nonlinearites of the circuit do not dominate. Like the previous modulator, the noise flattens out. In this second modulator it flattens out at a little bit lower frequency though - between 1/128 and 1/64 of the sampling frequency. This corner frequency corresponds to the pole of each integrator. Most likely the reason this pole is lower is that the casode current sources are better in the second circuit.

The DC component is not considered part of the signal or noise-plus-distortion in the signal-to-noise-plus-distortion calculations. The results of the signal-to-noise-plus-distortion calculations are shown in Table 4.1.

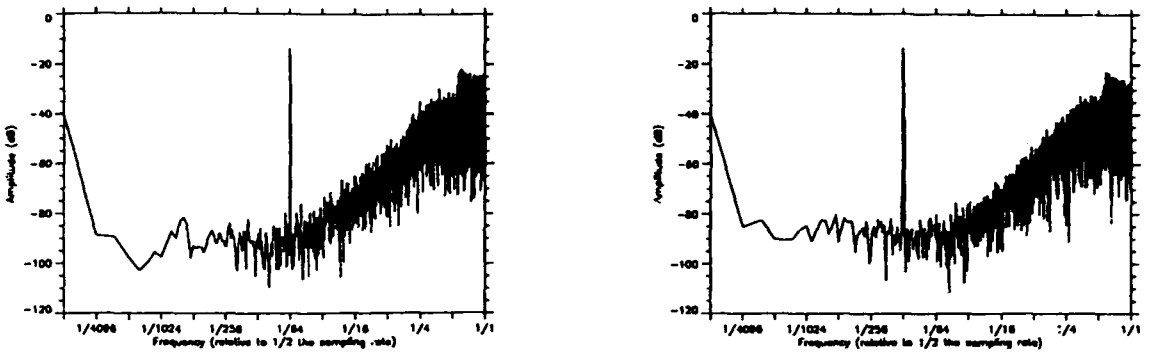


Figure 4.20. Frequency spectrums of half-scale 4 MHz and 2 MHz inputs.

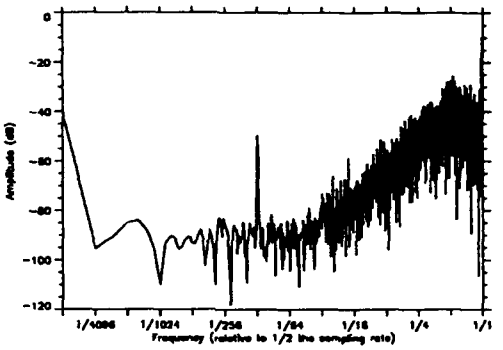


Figure 4.21. Frequency spectrum of 1/128-scale 2 MHz input.

Table 4.1. Resolution for various inputs.

Oversampling ratio	Signal to noise plus distortion (1/2-scale, 4 MHz)	Signal to noise plus distortion (1/2-scale, 2 MHz)	Signal to noise plus distortion (1/128-scale, 2 MHz)	Estimated dynamic range (1/128-scale, 2 MHz)
128	-	674 (9.3 bits)	14.8	1894 (10.9 bits)
64	655 (9.4 bits)	507 (9.0 bits)	10.1	1293 (10.3 bits)
32	338 (8.4 bits)	304 (8.2 bits)	5.65	723 (9.5 bits)
16	92 (6.5 bits)	103 (6.7 bits)	1.37	175 (7.5 bits)

5. Sigma-Delta Filter

The purpose of the sigma-delta filter is to remove noise outside the bandwidth of interest and to decimate the signal down to the Nyquist rate. The sigma-delta filter of this project, uses multiple stages. The stages of the filter are shown in Figure 5.1. The reason for choosing a multi-stage filter is because the first stage sinc filter is very simple and it reduces the clock rate tremendously. This reduction in clock rate makes it easier for the second stage of the filter to be implemented. Because the first stage of the filter is so simple, there is amplitude distortion. The second stage of the filter corrects this distortion and filters out any remaining noise so that the signal can be decimated down to the Nyquist rate.

5.1. Sinc Decimation Filter

One reason for using the sinc decimation filter is the simplicity of it. The filter coefficients can easily be implemented exactly and no multipliers are needed. Another reason for using the sinc decimation filter is that its response is well suited for removing the high frequency noise generated from the sigma-delta modulator. The sinc decimation filter is an easy way to reduce the sampling rate from a sigma-delta modulator by a factor of D, where D is no more than the oversampling rate R of the modulator. In this design, D was chosen to be 16 (half of the oversampling rate).

Before analyzing the sinc decimation filter used in the sigma-delta filter, a first-order sinc decimation filter will be analyzed. Before decimation, the first-order sinc fil-

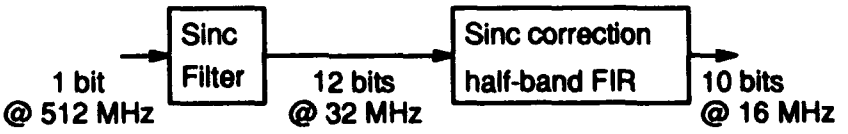


Figure 5.1. Stages of the filter.

ter has a transfer function of

$$H = \frac{1}{D}\sum_{i=0}^{D-1} z^{-i} = \frac{1}{D}\frac{1-z^{-D}}{1-z^{-1}} \tag{5.1}$$

and its frequency response is

$$|H| = \left|\frac{1}{D}\frac{\sin(D\pi fT)}{\sin(\pi fT)}\right| \approx \left|sinc(D\pi fT)\right| \tag{5.2}$$

From the above result, it can be seen why this filter is called a sinc filter. Its frequency response is basically an aliased sinc function. It can also be called an averaging filter because it takes the mean of the last D values as seen in (5.1).

The discrete time domain input-output relationship of the first-order sinc filter is

$$y(k) = \frac{1}{D}\sum_{i=0}^{D-1} x(k-i) \tag{5.3}$$

For the following analysis the input function will be assumed to have the property of

$$x(k) = 0, k \neq \left\lfloor\frac{k}{D}\right\rfloor D \tag{5.4}$$

The input function may have a non-zero value once every D points. The z-transform of this input function is then only a function of z^D. With this input, the output will be

$$y(k) = \frac{1}{D}x\left(\left\lfloor\frac{k}{D}\right\rfloor D\right) \tag{5.5}$$

This function has a stepping characteristic. It keeps a constant value over an interval of D points and then steps to another value over D points. The decimated output is defined as

$$y'(k) \equiv \begin{cases} Dy(k), k = \left\lfloor\frac{k}{D}\right\rfloor D \\ 0, k \neq \left\lfloor\frac{k}{D}\right\rfloor D \end{cases} \tag{5.6}$$

In this definition, one out of every D values are kept. The value that is kept is multiplied by the number of values it represents (D). With this definition, the decimated output is

$$y'(k) = x(k) \tag{5.7}$$

The output of the first-order sinc decimation filter is simply the input if the input is non-zero only once every D points. If an offset is used in (5.4) and/or (5.6), the same result occurs except that the output is be delayed.

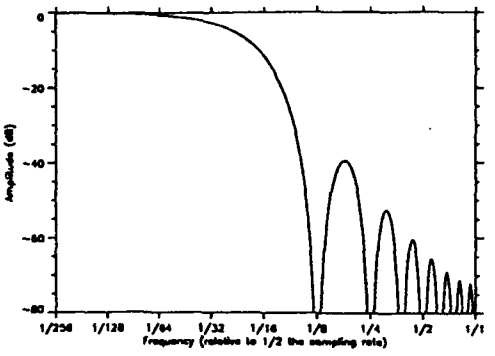


Figure 5.2. Sinc^3 frequency spectrum.

The sinc decimation filter used in the sigma-delta filter is one order higher than the order of the modulator. In this project, two second-order modulators were designed so a third-order sinc-decimation filter was needed. In [17], an analysis of different orders of the sinc filter relative to the order of the modulator is given. In this paper it is concluded that an order higher (M+1) is the best. The following analysis uses a more direct approach to this order of the sinc decimation filter.

The transfer function of the sinc filter before decimation is

$$H^{M+1} = \left(\frac{1}{D}\sum_{i=0}^{D-1} z^{-i}\right)^{M+1} = \left(\frac{1}{D}\frac{1-z^{-D}}{1-z^{-1}}\right)^{M+1} \tag{5.8}$$

The frequency response of the third-order sinc filter is shown in Figure 5.2. The noise from the modulator to be filtered is

$$N_1 = \left(1-z^{-1}\right)^M E \tag{5.9}$$

The noise after the sinc filter before decimation is then

$$N_2 = N_1 H^{M+1} = \left(\frac{1-z^{-D}}{D}\right)^M \left(\frac{1}{D}\frac{1-z^{-D}}{1-z^{-1}}\right) = \left(\frac{1-z^{-D}}{D}\right)^M H \tag{5.10}$$

The left part of this expression matches the qualification in (5.4) because it is only a function of z^D. Using (5.7), the decimated noise output of the sinc decimation filter is

$$N_3 = \left(\frac{1-z^{-D}}{D}\right)^M \tag{5.11}$$

The sinc filter causes some signal attenuation in the bandwidth. If this is to be compensated for in a later filter stage, the noise within the bandwidth after compensation would

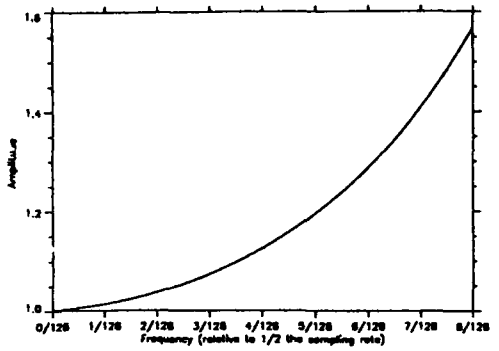


Figure 5.3. Extra noise after decimation and correction.

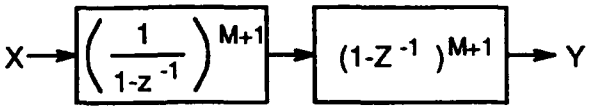


Figure 5.4. Structure of the sinc decimation filter.

be

$$N_4 = N_3 H^{-(M+1)} = N_1 H^{-1} \tag{5.12}$$

The final noise is increased by the inverse of a first-order sinc function. Figure 5.3 shows this increase over the decimated frequency range. For an oversampling ratio of 32 and decimation of 16, the noise amplification at the edge of the bandwidth is about 1.1 so little resolution is lost. When the oversampling ratio is equal to the decimation ratio, the amplification at the edge of the bandwidth is about 1.6 so about a bit of resolution may be lost.

The structure of the sinc decimation filter is shown in Figure 5.4. This structure can be implemented with M+1 accumulators and M+1 subtractors with delays. The scaling by $D^{-(M+1)}$ can be done by just a change in representation because D is a power of 2. In this structure the decimation is done in middle instead of at the end. In [18], it is shown that this position of decimation makes a filter that is equivalent to a filter that decimates at the end. The new decimated variables are

$$Z \equiv z^D \tag{5.13}$$

$$F \equiv fD \tag{5.14}$$

$$K \equiv \frac{k}{D} \tag{5.15}$$

A concern in the structure of Figure 5.4 is that the accumulators are not stable and they overflow for DC inputs. Because of this, it may appear that an infinite number

of bits are needed for these accumulators. If the overflow arithmetic of accumulators and subtractors use a modulo system such as two's complement, then the correct output of the filter can occur.

Using the following definition as the residue of a modulo b,

$$\langle a \rangle_b \equiv a - \left\lfloor \frac{a}{b} \right\rfloor b \tag{5.16}$$

one can easily derive

$$\left\langle \sum_i \langle a_i \rangle_b \right\rangle_b = \left\langle \sum_i a_i \right\rangle_b \tag{5.17}$$

From this, the output of the sinc filter with registers B bits wide is

$$y(k) = \left\langle \sum_{i_1=0}^{D-1} \sum_{i_2=0}^{D-1} \cdots \sum_{i_{M+1}=0}^{D-1} x\left(k - i_1 - i_2 \cdots - i_{M+1}\right) \right\rangle_{2^B} \tag{5.18}$$

This output gives the same output as a sinc filter which has infinite size registers only if the maximum value of the summation does not overflow. Knowing that the input to the filter is a bit stream, the sinc filter output does not overflow when

$$2^B > D^{M+1} \tag{5.19}$$

If the largest state (input is one for $(M+1)D$ cycles) is assumed not to occur, then the number of bits needed is

$$B = (M+1)\log_2 D \tag{5.20}$$

This is 12 for a second-order modulator and a decimation of 16.

5.2. FIR half-band correction filter

A problem with the sinc decimation filter is that it causes some signal attenuation. Something must compensate for this for the filter to give accurate resolution. One solution is to have the modulator compensate by having an integrator gain such that additional transfer function in (2.13) or (4.5) cancel out the sinc attenuation. Another solution would be to have an IIR filter after the sinc filter which did the compensation [18,19]. A third solution would be to have an FIR filter after the sinc filter do the compensation [18,20].

Also needed after the sinc decimation filter is another filter because the decimation done is only half of the oversampling ratio. A half-band filter is needed to filter out the remaining noise so that the signal can be decimated down to the Nyquist rate. Like the compensator there are IIR and FIR solutions [18]. Other solutions include wave

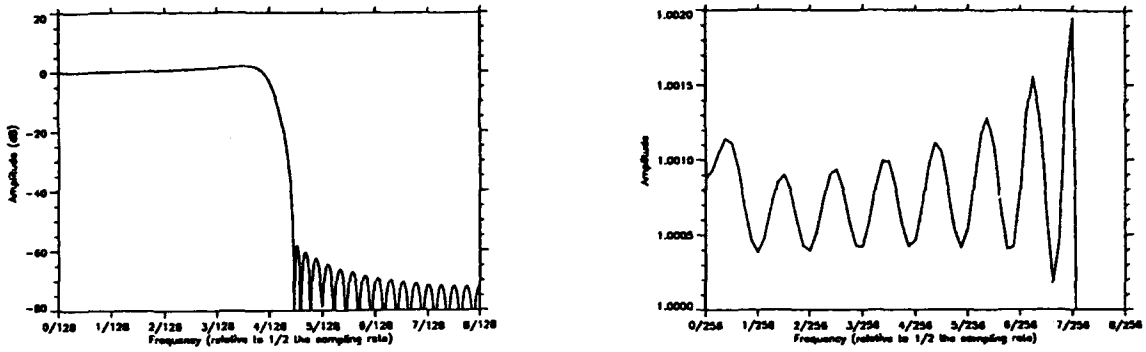


Figure 5.5. FIR spectrum and the passband spectrum of both filter stages.

filters [19] and multiplier-free filters [20]. Both the compensation and half-band filtering can be done in software or a DSP using the same algorithms provided the output from the modulator can be stored and processed later.

In this project, a single stage filter is used for compensation and half-band filtering. An FIR filter is used so that no phase distortion occurs. The ideal frequency response from 0 to $2FT$ of the filter is

$$H' = \begin{cases} \left[D\frac{\sin\frac{\pi FT}{D}}{\sin(\pi FT)}\right]^3, 2FT < \frac{1}{2} \\ 0, 2FT > \frac{1}{2} \end{cases} \tag{5.21}$$

Using an inverse z-transform, the filter coefficients are

$$h'(K) = T\int_{\frac{-1}{2T}}^{\frac{1}{2T}} H' e^{j2FTK\pi} dF = 2T\int_{0}^{\frac{1}{2T}} H' \cos(2FTK\pi) dF \tag{5.22}$$

For a real filter only a finite number of coefficients can be used and the filter must be causal. The real filter coefficients are

$$h(K) = h'\left(K - \left\lfloor\frac{N}{2}\right\rfloor\right), 0 \le K < N \tag{5.23}$$

where N is 65 for this project. Numerical integration is used to find these coefficients. Figure 5.5 shows the frequency response of the FIR filter and the passband of the total filter showing how the FIR filter compensated for the sinc attenuation.

5.3. Simulation and Results

PV-WAVE was used to simulate the filtering of the output of each of the sigma-delta modulator. Functions were written for PV-WAVE to generate both filter stages

including the filter coefficients. Functions were also written to process data by arbitrary filters. The frequency spectrums of the modulator signal after the sinc decimation filter and at the final output of the filter are shown in Figures 5.6 and 5.7. The signal resolution at these points are shown in Tables 5.1 and 5.2.

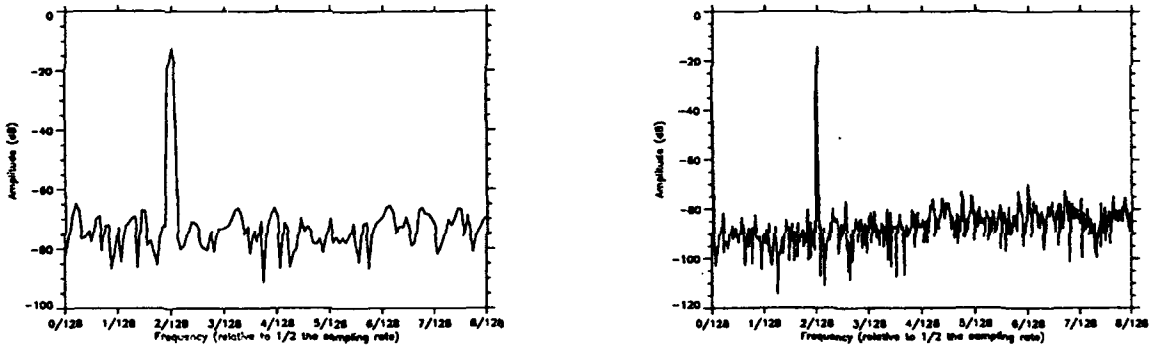


Figure 5.6. Output of the sinc decimation filter for modulator #1 and #2.

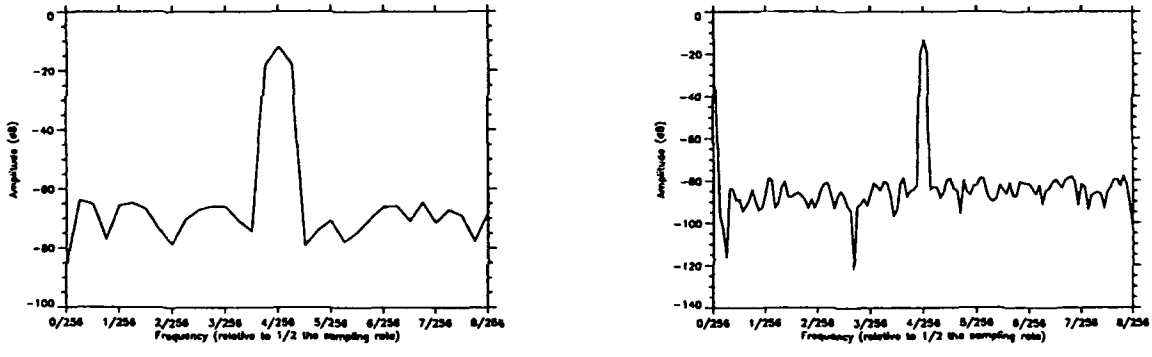


Figure 5.7. Output of the FIR filter after decimation for modulator #1 and #2.

Table 5.1. Resolution after the sinc decimation filter.

Modulator	Signal to noise plus distortion	Estimated dynamic range
#1	98 (6.6 bits)	263 (8.0 bits)
#2	151 (7.2 bits)	314 (8.3 bits)

Table 5.2. Resolution after final decimation.

Modulator	Signal to noise plus distortion	Estimated dynamic range
#1	151 (7.2 bits)	596 (9.2 bits)
#2	354 (8.5 bits)	850 (9.7 bits)

6. Conclusion

The design, simulation, and analysis of two GaAs second-order sigma-delta modulators used for an analog-to-digital converter have been presented. Also presented was a partial design and simulation of a filter to be used with the two sigma-delta modulators.

Both of the modulators contain some unique circuits. Two different non-standard continuous time integrators were used in these modulators. The first modulator used the square law of FETs to create the integrators. The second modulator used operational amplifiers and current sources to create integrators which have a small capacitive input load.

The two modulators designed in this project were modeled in the discrete-time domain even though continuous time integrators were used. In the first modulator a special clocking scheme was used to accomplish this. In the second modulator, an extra transfer function was used as part of the model for the integrator. In both modulators, the integrators were clocked in such a way that they were made insensitive to the quantizer delay.

To filter the sigma-delta modulator output, a two-stage filter was used. The first stage is a sinc filter and seems to be ideally suited for the sigma-delta modulator. It filters out most of the noise and decimates the signal down to twice the Nyquist rate. The second-stage of the filter corrects attenuation caused by the sinc filter and filters out the remaining noise so that the final decimation can occur.

These two modulators are clocked at 512 MHz and have an oversampling ratio of 32 for the bandwidth of interest (8 MHz). The first modulator achieves a resolution of 8-9 bits after filtering. The second modulator achieves a resolution of 9-10 bits after filtering. The final output word rate for both modulators is 16 Msamples/s. The second modulator is about a bit better than the first modulator for the bandwidth chosen.

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